AKD4641EN-A
Evaluation board Rev.1 for AK4641EN

GENERAL DESCRIPTION

The AKD4641 is an evaluation board for the AK4641, 16bit stereo CODEC with built-in Microphone-amplifier and 16bit Mono CODEC for Bluetooth Interface. The AKD4641 can evaluate A/D converter and D/A converter separately in addition to loopback mode (A/D → D/A). The AKD4641 also has the digital audio interface and can achieve the interface with digital audio systems via opt-connector.

■ Ordering guide

AKD4641EN-A --- Evaluation board for AK4641EN
(Cable for connecting with printer port of IBM-AT, compatible PC and control software are packed with this. This control software does not support Windows NT.)

FUNCTION

- **DIT/DIR with optical input/output**
- **BNC connector for an external clock input**
- **10pin Header for I²C control mode**
- **On board headphone-amp (MAX4410) and speaker-amp (LM4889)**

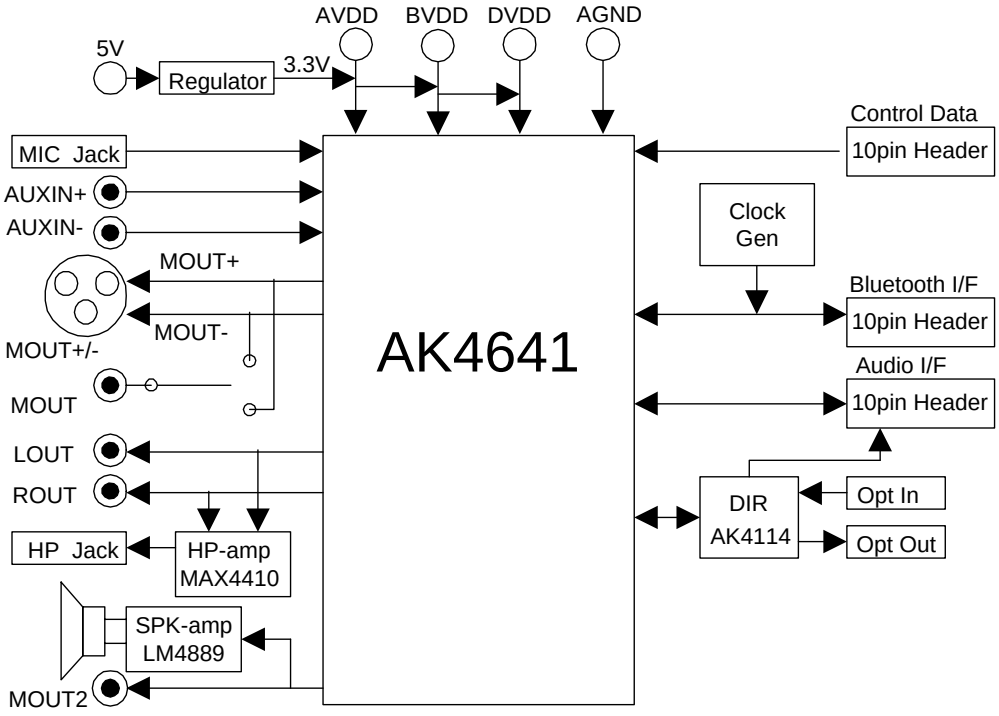


Figure 1. AKD4641 Block Diagram

* Circuit diagram and PCB layout are attached at the end of this manual

Evaluation Board Manual

■ Operation sequence

1) Set up the power supply lines.

1-1) When AVDD, BVDD, DVDD and VCC are supplied from the regulator. (AVDD, BVDD, DVDD and VCC jack should be open.). See "**Other jumper pins set up** (page 9)". <default>

[REG]	(red)	= 5V	
[AVDD]	(orange)	= open	: 3.3V is supplied to AVDD of AK4641 from regulator.
[BVDD]	(orange)	= open	: 3.3V is supplied to BVDD of AK4641 from regulator.
[DVDD]	(orange)	= open	: 3.3V is supplied to DVDD of AK4641 from regulator.
[VCC]	(orange)	= open	: 3.3V is supplied to logic block from regulator.
[H/SVDD]	(orange)	= 3.3V	: for MAX4410 and LM4889 logic (typ.3.3V)
[AGND]	(black)	= 0V	: for analog ground
[DGND]	(black)	= 0V	: for logic ground

1-2) When AVDD, BVDD, DVDD and VCC are not supplied from the regulator. (AVDD, BVDD, DVDD and VCC jack should be open). See "**Other jumper pins set up** (page 9)".

[REG]	(red)	= "REG" jack should be open.	
[AVDD]	(orange)	= 2.6 ~ 3.6V	: for AVDD of AK4641 (typ. 3.3V)
[BVDD]	(orange)	= 2.6 ~ 3.6V	: for BVDD of AK4641 (typ. 3.3V)
[DVDD]	(orange)	= 2.6 ~ 3.6V	: for DVDD of AK4641 (typ. 3.3V)
[VCC]	(orange)	= 2.6 ~ 3.6V	: for logic (typ. 3.3V)
[H/SVDD]	(orange)	= 2.6 ~ 3.6V	: for MAX4410 and LM4889 logic (typ.3.3V)
[AGND]	(black)	= 0V	: for analog ground
[DGND]	(black)	= 0V	: for logic ground

Each supply line should be distributed from the power supply unit.
DVDD and VCC must be same voltage level.

2) Set up the evaluation mode, jumper pins and DIP switches. (See the followings.)

3) Power on.
The AK4641 and AK4114 should be reset once bringing SW1, 2 "L" upon power-up.

■ Evaluation mode

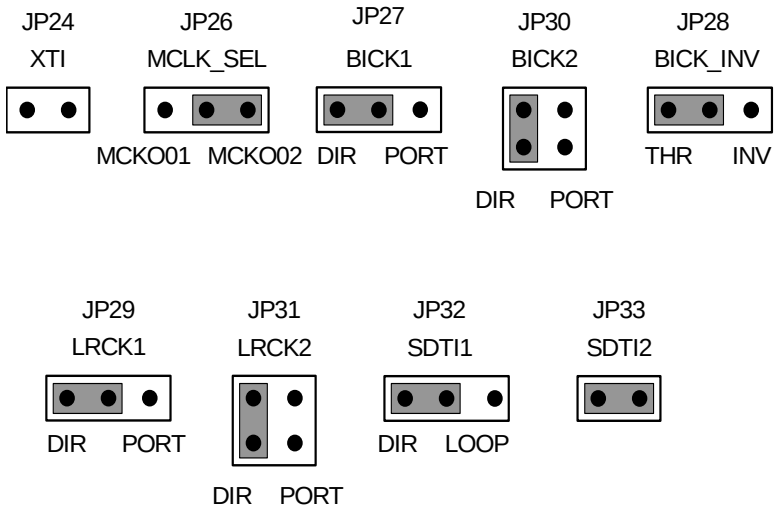
1. Evaluation of 16bit stereo CODEC

In case of AK4641 evaluation using AK4114, it is necessary to correspond to audio interface format for AK4641 and AK4114. About AK4641's audio interface format, refer to datasheet of AK4641. About AK4114's audio interface format, refer to Table 2 in this manual.

(1-1) Evaluation of Recording block (MIC, ADC) using DIT of AK4114
(1-2) Evaluation of Playback block (HP, SPK, MOUT) using DIR of AK4114
(1-3) Evaluation of Loop Back (ADC → DAC) using 16bit Mono CODEC <default>
(1-4) All interface signals including master clock are fed externally.

(1-1) Evaluation of Recording block (MIC, ADC) using DIT of AK4114

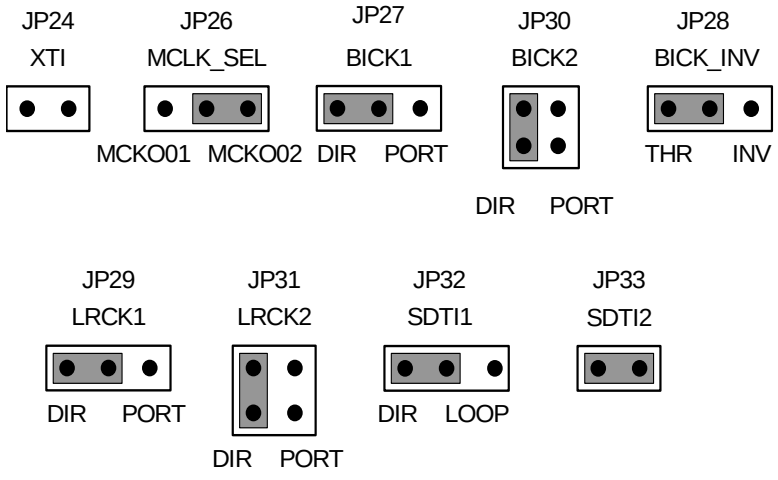
PORT2 (DIT) and X2 (X'tal) are used. DIT generates audio bi-phase signal from received data and which is output through optical connector (TOTX141). Nothing should be connected to PORT1 (DIR) and PORT3 (Audio I/F), J12 (EXT). JP25 (EXT) is short. CM0 is set "H " and CM1 is set "L " for SW1, AK4114 is set X'tal mode.



DIT does not operate under fs = 32kHz, this mode corresponds to fs = 32kHz and over.

(1-2) Evaluation of Playback block (HP, SPK, MOUT) using DIR of AK4114

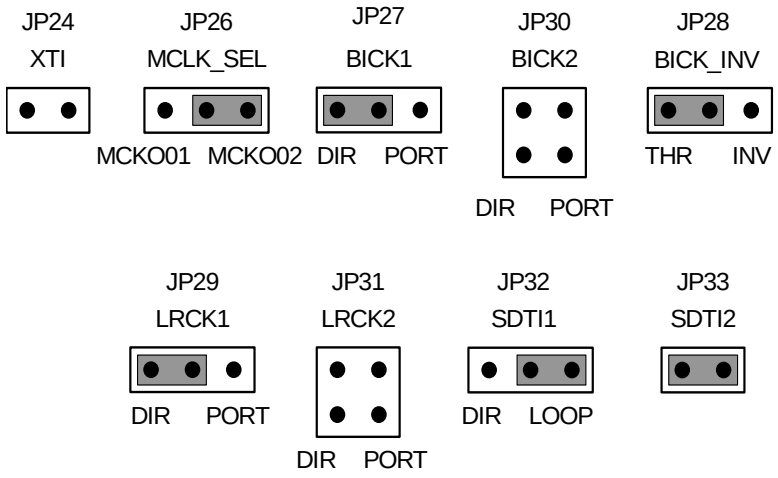
PORT1 (DIR) is used. Nothing should be connected to PORT3 (Audio I/F) and J12 (EXT). X1 (X'tal) is removed. JP25 (EXT) is short. CM0 is set "L " and CM1 is set "L " for SW1, AK4114 is set PLL mode.



DIR does not operate under fs = 32kHz, this mode corresponds to fs = 32kHz and over.

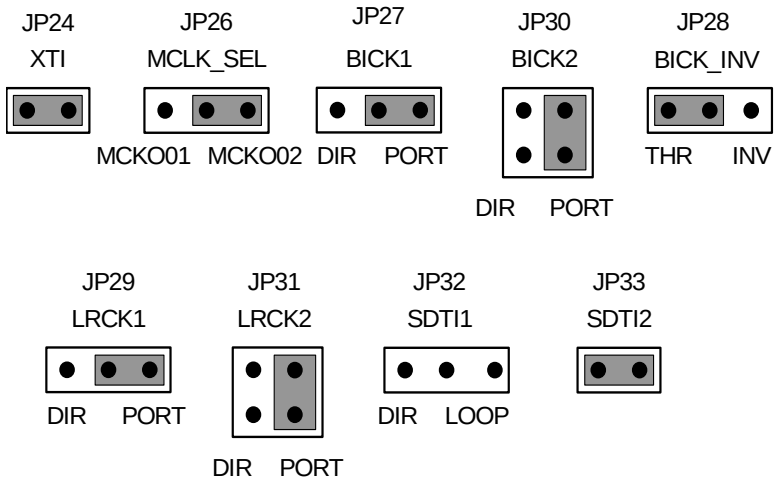
(1-3) Evaluation of Loop Back (ADC → DAC) using 16bit Mono CODEC <default>

X2 (X'tal) is used. Nothing should be connected to PORT1 (DIR), PORT2 (DIT) and PORT3 (Audio I/F).



(1-4) All interface signals including master clock are fed externally.

PORT3 (Audio I/F) and J12 (EXT) is used. Nothing should be connected to PORT1 (DIR). X2 (X'tal) is removed. JP25 (EXT) and R51 should be properly selected in order to much the output impedance of the clock generator.



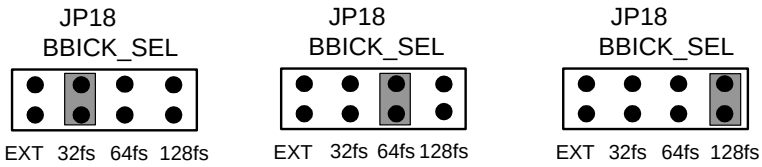
JP28 (BICK_INV) is jumper which decides polarity of BICK, set "THR" or "INV" for audio interface format.

2. Evaluation of 16bit Mono CODEC

(2-1) Set up jumper pins of BBICK clock
(2-2) Set up jumper pins of BSYNC clock
(2-3) Set up jumper pins of two types of data formats
(2-4) Evaluation of ADC (AUXIN) using 16bit Mono CODEC
(2-5) Evaluation of DAC (MOUT) using 16bit Mono CODEC
(2-6) Evaluation of Loop Back (ADC → DAC) using 16bit Mono CODEC <default>

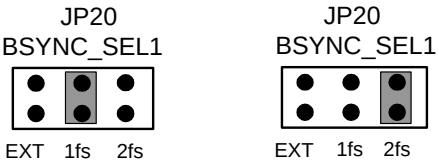
(2-1) Set up jumper pins of BBICK clock

Input frequency of BBICK can be set up in turn “32fs”,”64fs” or “128fs” from left.



(2-2) Set up jumper pins of BSYNC clock

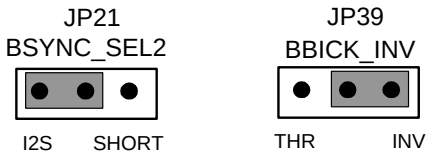
Input frequency of BSYNC can be set up in turn “2fs” or “1fs” from left.



When an external clock through a BNC connector (J10: BBICK and J11: BSYNC) is supplied, select EXT on JP18 (BBICK_SEL) and JP20 (BSYNC_SEL) and short JP17 (XTE). JP22 (EXT1) and JP23 (EXT2) and R44 and R45 should be properly selected in order to much the output impedance of the clock generator.

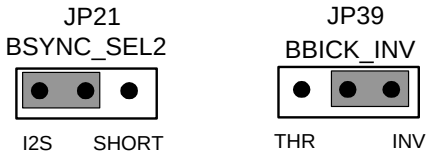
(2-3) Set up jumper pins of two types of data formats

(2-3-1) Set up jumper pins of “I2S” <default>



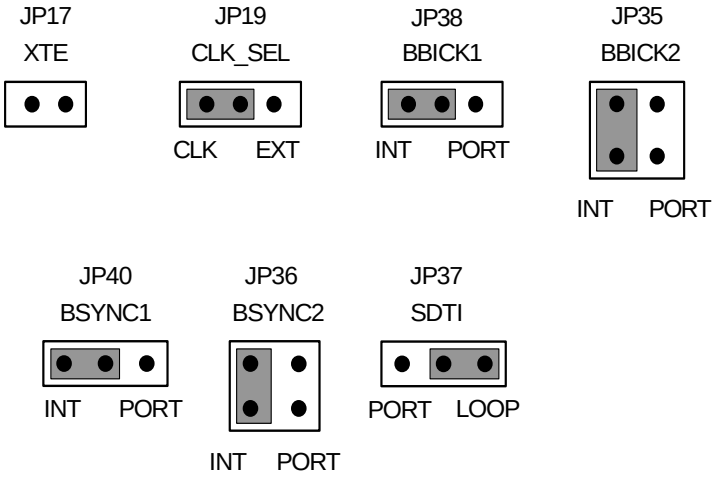
(2-3-2) Set up jumper pins of “Short Format Sync”

(2-3-3) Set up jumper pins of “MSB justified”



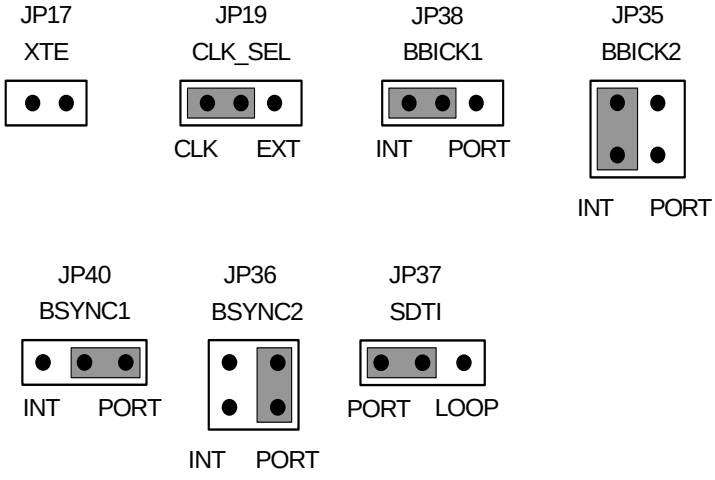
(2-4) Evaluation of ADC (AUXIN) using 16bit Mono CODEC

PORT5 (Bth I/F) and X1 (X’tal) are used. Nothing should be connected to J10 (BBICK) and J11 (BSYNC).



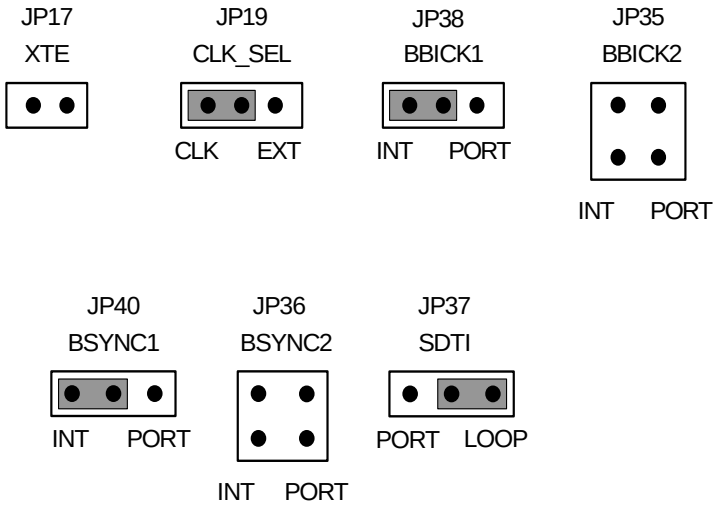
(2-5) Evaluation of DAC (MOUT) using 16bit Mono CODEC

PORT5 (Bth I/F) and X1 (X’tal) are used. Nothing should be connected to J10 (BBICK) and J11 (BSYNC).
When an BSYNC through a PORT5 connector (Bth I/F) is supplied, open JP20 (BSYNC_SEL).



(2-6) Evaluation of Loop Back (ADC → DAC) using 16bit Mono CODEC

X1 (X'tal) are used. Nothing should be connected to PORT5 (Bth -I/F), J10 (BBICK) and J11 (BSYNC).



■ DIP Switch set up

[SW1] : Mode Setting of AK4114
ON is “H”, OFF is “L”.

No.	Name	ON (“H”)	OFF (“L”)	Default
1	DIF0	AK4114 Audio Format Setting See Table 2		ON
2	DIF2			ON
3	CM0	AK4114 AUTO (X’tal / PLL) Mode		OFF
4	CM1			ON
5	OCKS1	Fixed to “L”		OFF
6	TST2			OFF
7	NC			OFF

Table 1. Mode Setting for AK4534 and AK4114

Mode	DIF2	DIF0	AK4114 DAUX	AK4114 SDTO
0	0	0	24bit, MSB justified	16bit, LSB justified
1	0	1	24bit, MSB justified	24bit, LSB justified
2	1	0	24bit, MSB justified	24bit, MSB justified
3	1	1	24bit, I^2S	24bit, I^2S

Table 2. Setting for AK4114 Audio Interface Format

Mode	CM1	CM0	UNLOCK	PLL	X'tal	Clock source	SDTO
0	0	0	-	ON	ON(Note)	PLL	RX
1	0	1	-	OFF	ON	X'tal	DAUX
2	1	0	0	ON	ON	PLL	RX
			1	ON	ON	X'tal	DAUX
3	1	1	-	ON	ON	X'tal	DAUX

ON: Oscillation (Power-up), OFF: STOP (Power-down)
Note : When the X’tal is not used as clock comparison for fs detection (i.e. XTL1,0= “1,1”), the X’tal is off.

Table 3. Clock Operation Mode select

No.	OCKS1	MCKO1	MCKO2	X’tal	fs (max)
0	0	256fs	256fs	256fs	96 kHz
2	1	512fs	256fs	512fs	48 kHz

Table 4. Master Clock Frequency Select (Stereo mode)

■ Other jumper pins set up

1. JP1 (GND): Analog ground and Digital ground
   OPEN : Separated. <default>
   SHORT: Common. (The connector “DGND” can be open.)

2. JP3 (AVDD_SEL): AVDD of the AK4641
   REG : AVDD is supplied from the regulator (“AVDD” jack should be open). < default >
   AVDD : AVDD is supplied from “AVDD ” jack.

3. JP4 (BVDD_SEL): BVDD of the AK4641
   AVDD : AVDD is supplied from “AVDD”. < default >
   BVDD : BVDD is supplied from “BVDD ” jack.

4. JP5 (DVDD_SEL): BVDD of the AK4641
   BVDD : DVDD is supplied from “BVDD”. < default >
   DVDD : BVDD is supplied from “BVDD ” jack.

5. JP2 (D3.3V_SEL): VCC of logic
   DVDD : VCC is supplied from “DVDD”. < default >
   VCC : VCC is supplied from “VCC ” jack.

6. JP6 (LOUT/HP_SEL): Select analog signal of LOUT pin
   LOUT : Analog signal of LOUT pin is output from J1 (RCA) connector. < default >
   ROUT : Analog signal of LOUT pin is output from J2 (mini jack) connector.

7. JP7 (ROUT/HP_SEL): Select analog signal of ROUT pin
   LOUT : Analog signal of LOUT pin is output from J1 (RCA) connector. < default >
   ROUT : Analog signal of LOUT pin is output from J2 (mini jack) connector.

8. JP8 (SHDN_L): Left-Channel shutdown mode for MAX4410
   OPEN : Left-Channel active mode.
   SHORT: Left-Channel shutdown mode. < default >

9. JP9 (SHDN_R): Right-Channel shutdown mode for MAX4410
   OPEN : Right-Channel active mode.
   SHORT: Right-Channel shutdown mode. < default >

10. JP12 (MOUT2/SPK_SEL): Select analog signal of MOUT2 pin
    MOUT2 : Analog signal of MOUT2 pin is output from J7 (RCA) connector. < default >
    SPK : Analog signal of MOUT2 pin is output from speaker.

11. JP15 (SHDN_SPK): shutdown mode for LM4889
    OPEN : Speaker active mode.
    SHORT: Speaker shutdown mode. < default >

12. JP34 (BSDTO): Please make use of open < default >

■ The function of the toggle SW

Upper-side is “H” and lower-side is “L”.

[SW1] (DIR): Power down of the AK4114. Keep “H” during normal operation.

Keep “L” when the AK4114 is not used.

[SW2] (PDN): Power down of the AK4641. Keep “H” during normal operation.

■ Indication for LED

[LED1] (ERF): Monitor INT0 pin of the AK4114. LED turns on when the AK4114 has some error.

■ I²C- bus Control Interface

The AK4641 can be controlled via the printer port (parallel port) of IBM-AT compatible PC. Connect PORT4 (CTRL) with PC by 10 wire flat cable packed with the AKD4641.

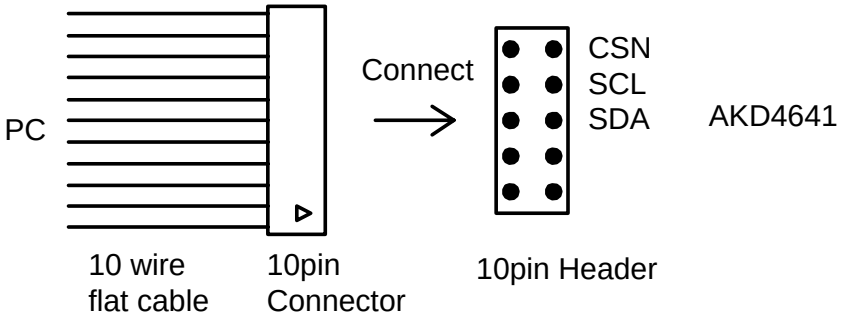


Figure 2. Connect of 10 wire flat cable

■ Analog Input / Output Circuits

1. Input Circuits

1-1. MIC Input Circuit

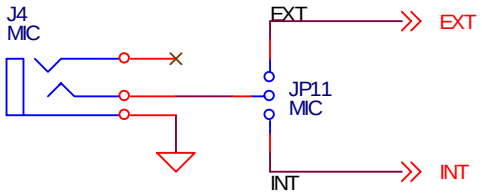
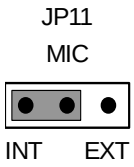
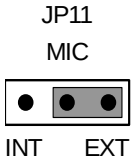


Figure 3. MIC Input Circuit

(1) Analog signal is input to INT pin via J4 connector. <default>



(2) Analog signal is input to EXT pin via J4 connector.



1-2. AUXIN+ / AUXIN- Input Circuit

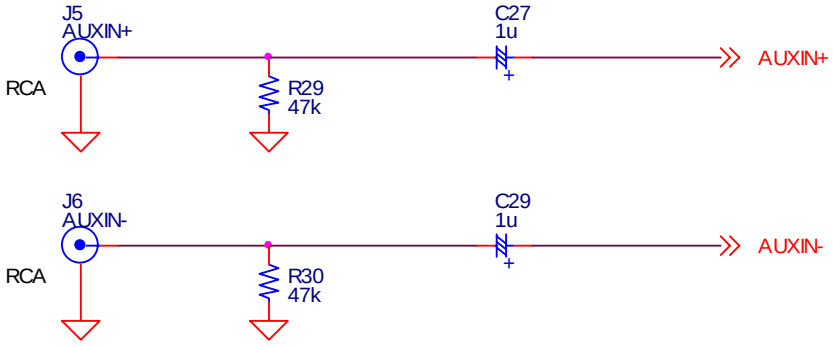


Figure 4. AUXIN+ / AUXIN- Input Circuits

2. Output Circuits

2-1. LOUT / ROUT Output Circuit

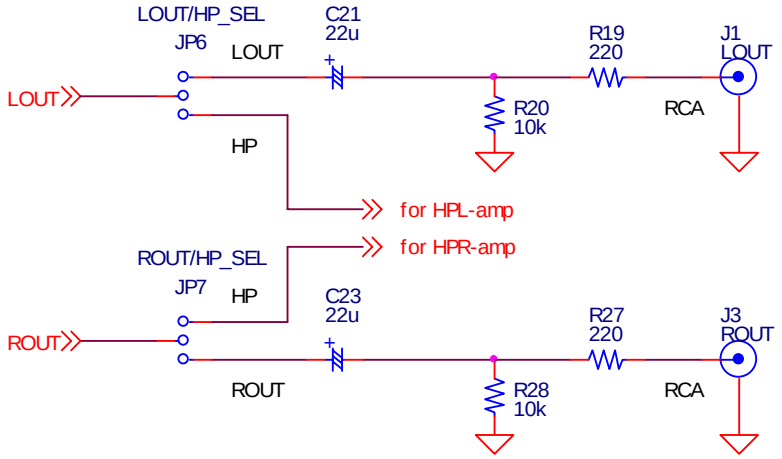


Figure 5. LOUT /ROUT Output Circuit

2-2. MOUT2 Output

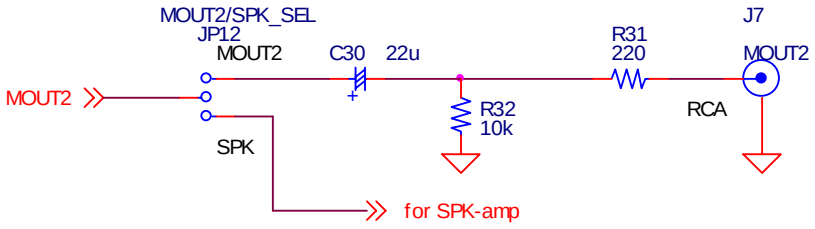


Figure 6. MOUT2 Output Circuit

2-3. MOUT+/– Output Circuit

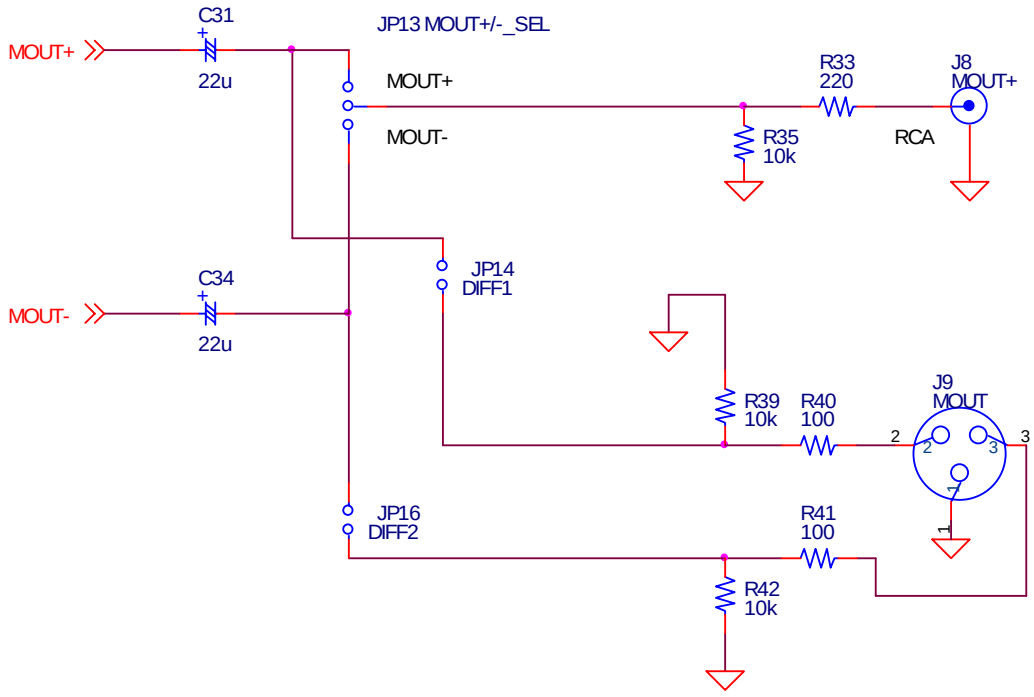
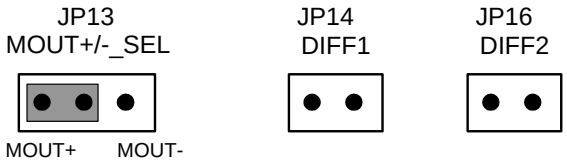
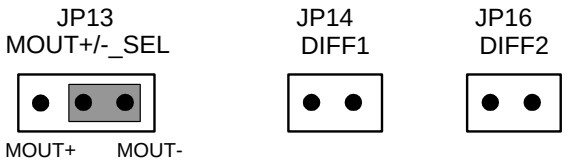


Figure 7. MOUT+/– Output Circuit

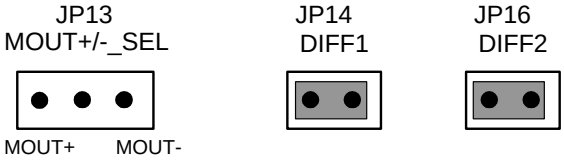
(1) Signal of MOUT+ pins are output from J8.



(2) Signal of MOUT– pins are output from J8.



(3) Signal of MOUT+ / - pins are output from J9. <default>



∗ AKM assumes no responsibility for the trouble when using the above circuit examples.

Control Software Manual

■ Set-up of evaluation board and control software

This evaluation board supports to I^2C control.

1. Set up the AKD4641 according to previous term.

2. Connect IBM-AT compatible PC with AKD4641 by 10-line type flat cable (packed with AKD4641). Take care of the direction of 10pin header. (Please install the driver in the CD-ROM when this control software is used on Windows 2000/XP. Please refer "Installation Manual of Control Software Driver by AKM device control software". In case of Windows95/98/ME, this installation is not needed. This control software does not operate on Windows NT.)

3. Insert the CD-ROM labeled "AK4641 Evaluation Kit" into the CD-ROM drive.

4. Access the CD-ROM drive and double-click the icon of "akd4641.exe" to set up the control program.

5. Then please evaluate according to the follows.

■ Operation flow

Keep the following flow.

1. Set up the control program according to explanation above.
2. Click "Port Setup" button.
3. Click "Write default" button.
4. Then set up the dialog and input data.

■ Explanation of each buttons

1. [Port Reset] : Set up the port. When this is pushed, the printer port or USB port is selected automatically.
2. [Write default] : Initialize the register of the AK4641
3. [All Read] : Read all registers of the AK4641.
4. [All Write] : Write all registers that is currently displayed
5. [Function1] : Dialog to write data by keyboard operation.
6. [Function2] : Dialog to evaluate IPGA and ATTL/ATTR.
7. [Function3] : The sequence of register setting can be set and executed.
8. [Function4] : The sequence that is created on [Function3] can be assigned to buttons and executed.
9. [Function5] : The register setting that is created by [SAVE] function on main window can be assigned to buttons and executed.
10. [Write] : Dialog to write data by mouse operation.
11. [Read] : Read data by mouse operation.
12. [SAVE] : Save the current register setting.
13. [OPEN] : Write the save values to all register.

■ Indication of data

Input data is indicated on the register map. Red letter indicates "H" or "1" and blue one indicates "L" or "0". Blank is the part that is not defined in the datasheet.

■ Explanation of each dialog

1. [Function1 Dialog] : Dialog to write data by keyboard operation

Address Box: Input register address in 2 figures of hexadecimal.
Data Box: Input register data in 2 figures of hexadecimal.

If you want to write the input data to AK4641, click “OK” button. If not, click “Cancel” button.

2. [Function2 Dialog] : Dialog to evaluate IPGA and ATTL/ATTR

This dialog corresponds to only addr=0BH and 0CH, 0DH.

Address Box: Input register address in 2 figures of hexadecimal.
Start Data Box: Input start data in 2 figures of hexadecimal.
End Data Box: Input end data in 2 figures of hexadecimal.
Interval Box: Data is written to AK4641 by this interval.
Step Box: Data changes by this step.
Mode Select Box:

If you check this check box, data reaches end data, and returns to start data.
[Example] Start Data = 00, End Data = 09
Data flow: 00 01 02 03 04 05 06 07 08 09 09 08 07 06 05 04 03 02 01 00

If you do not check this check box, data reaches end data, but does not return to start data.
[Example] Start Data = 00, End Data = 09
Data flow: 00 01 02 03 04 05 06 07 08 09

If you want to write the input data to AK4641, click “OK” button. If not, click “Cancel” button.

3. [Write Dialog] : Dialog to write data by mouse operation

There are dialogs corresponding to each register.

Click the “Write” button corresponding to each register to set up the dialog. If you check the check box, data becomes “H” or “1”. If not, “L” or “0”.

If you want to write the input data to AK4641, click “OK” button. If not, click “Cancel” button.

4.[Save] and [Open]

4-1. [Save]

Save the current register setting data. The extension of file name is “akr”.

(Operation flow)
(1) Click [Save] Button.
(2) Set the file name and push [Save] Button. The extension of file name is “akr”.

4 -2. [Open]

The register setting data saved by [Save] is written to AK4643. The file type is the same as [Save].

(Operation flow)
(1) Click [Open] Button.
(2) Select the file (*.akr) and Click [Open] Button.

5.[Function3 Dialog]

The sequence of register setting can be set and executed.

(1) Click [F3] Button.
(2) Set the control sequence.
Set the address, Data and Interval time. Set “-1” to the address of the step where the sequence should be paused.
(3) Click [Start] button. Then this sequence is executed.

The sequence is paused at the step of Interval="-1". Click [START] button, the sequence restarts from the paused step.

This sequence can be saved and opened by [Save] and [Open] button on the Function3 window. The extension of file name is “aks”.

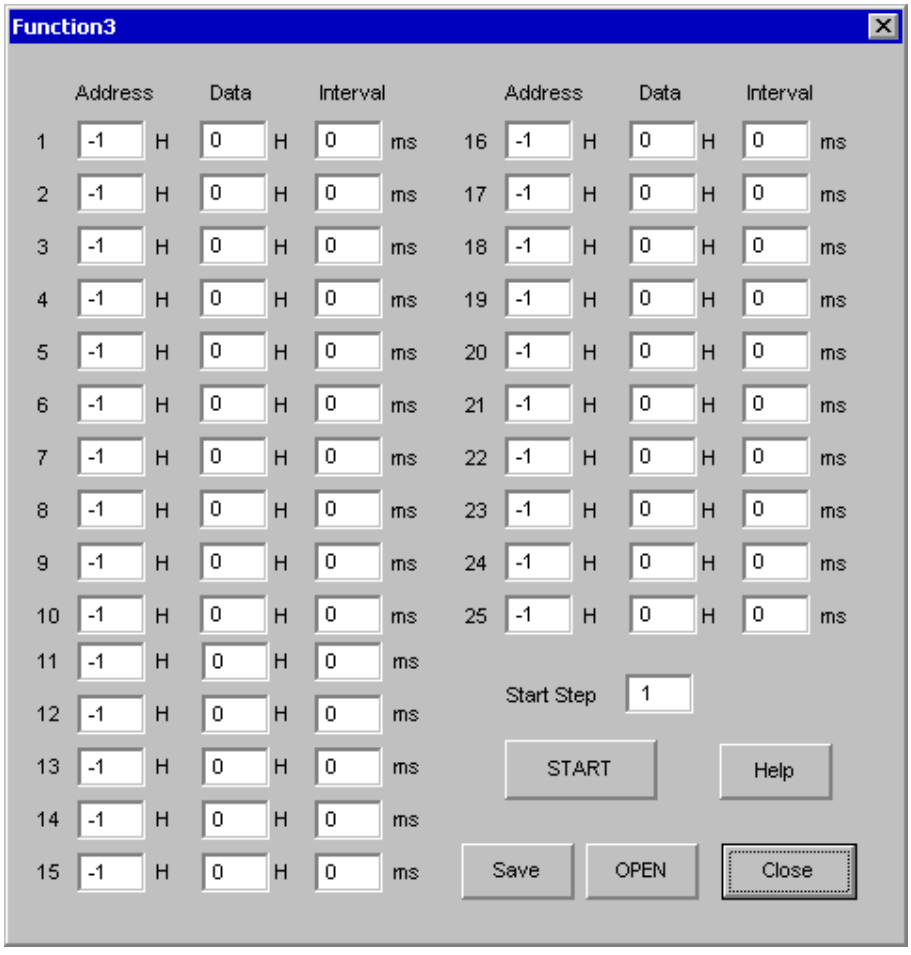


Figure 1. Window of [F3]

6. [Function4 Dialog]

The sequence that is created on [Function3] can be assigned to buttons and executed. When [F4] button is clicked, the window as shown in Figure2 opens.

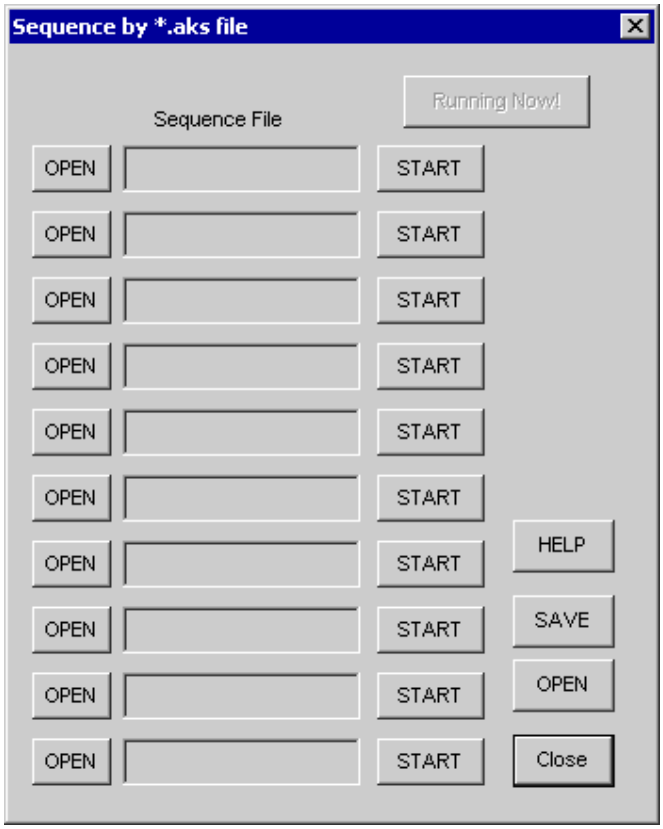


Figure 2. [F4] window

6-1. [OPEN] buttons on left side and [START] buttons

(1) Click [OPEN] button and select the sequence file (*.aks).

The sequence file name is displayed as shown in Figure 3.

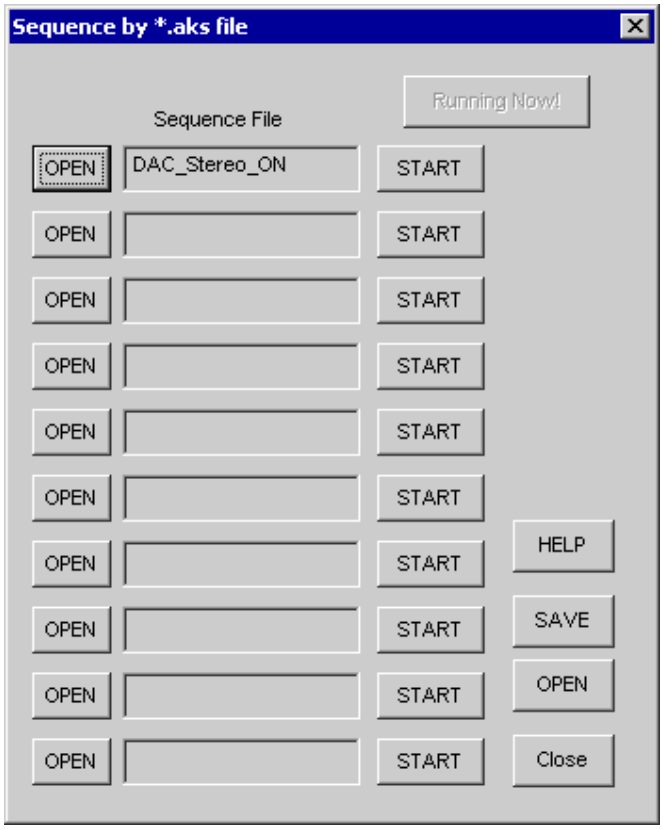


Figure 3. [F4] window(2)

(2) Click [START] button, then the sequence is executed.

6-2. [SAVE] and [OPEN] buttons on right side

[SAVE] : The sequence file names can assign be saved. The file name is *.ak4.
[OPEN] : The sequence file names assign that are saved in *.ak4 are loaded.

6-3. Note

(1) This function doesn't support the pause function of sequence function.
(2) All files need to be in same folder used by [SAVE] and [OPEN] function on right side.
(3) When the sequence is changed in [Function3], the file should be loaded again in order to reflect the change.

7.[Function5 Dialog]

The register setting that is created by [SAVE] function on main window can be assigned to buttons and executed. When [F5] button is clicked, the following window as shown in Figure 4 opens.

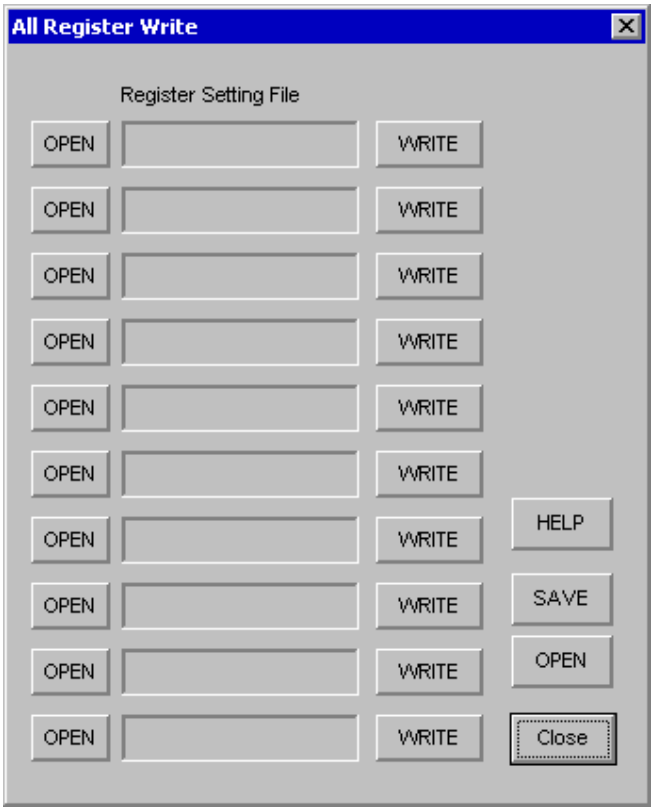


Figure 4. [F5] window

7-1. [OPEN] buttons on left side and [WRITE] button

(1) Click [OPEN] button and select the register setting file (*.akr).
The register setting file name is displayed as shown in Figure 5.
(2) Click [WRITE] button, then the register setting is executed.

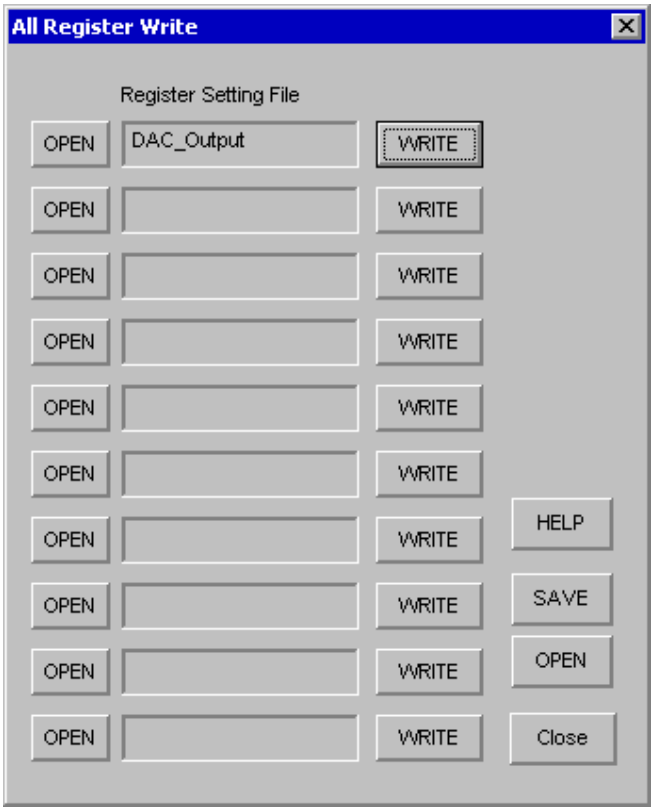


Figure 5. [F5] windows(2)

7-2. [SAVE] and [OPEN] buttons on right side

[SAVE] : The register setting file names assign can be saved. The file name is *.ak5.
[OPEN] : The register setting file names assign that are saved in *.ak5 are loaded.

7-3. Note

(1) All files need to be in same folder used by [SAVE] and [OPEN] function on right side.
(2) When the register setting is changed by [Save] Button in main window, the file should be loaded again in order to reflect the change.

Measurement Result

1. 16bit stereo CODEC

[Measurement condition]

- Measurement unit : Audio Precision, System Two
- MCLK : 256fs
- BICK : 64fs
- fs : 44.1kHz
- Bit : 16bit
- Power Supply : AVDD=BVDD=DVDD=3.3V
- Measurement Filter : 20Hz ~ 20kHz
- Temperature : Room

[Measurement Results]

1.ADC (INT) characteristics (MIC Gain = +20dB, IPGA = 0dB, ALC1 = OFF, MIC → IPGA → ADC)

		[dB]
THD+N	20kHzLPF (-1dB)	83.3
DR	20kHzLPF + A-weighted	86.1
S/N	20kHzLPF + A-weighted	86.1

2.ADC (EXT) characteristics (MIC Gain = +20dB, IPGA = 0dB, ALC1 = OFF, EXT → IPGA → ADC)

		[dB]
THD+N	20kHzLPF (-1dB)	83.3
DR	20kHzLPF + A-weighted	86.1
S/N	20kHzLPF + A-weighted	86.1

3. ADC (AUXIN+ / AUXIN-) characteristics (MICAD =0, AUXIN+/AUXIN- → ADC)

		[dB]
THD+N	20kHzLPF (-1dB)	87.6
DR	20kHzLPF + A-weighted	91.1
S/N	20kHzLPF + A-weighted	91.1

4. DAC (LOUT/ROUT) characteristics (R_L=10kΩ, DAC → LOUT/ROUT)

		L[dB]	R[dB]
THD+N	20kHzLPF (-3dB)	86.4	86.4
DR	20kHzLPF + A-weighted	89.4	89.5
S/N	20kHzLPF + A-weighted	90.7	91.0

5. DAC (MOUT+ / MOUT-) characteristics (R_L=20kΩ, DAC → MOUT+ / MOUT-)

		MOGN=0[dB]	MOGN=1[dB]
THD+N	20kHzLPF (-3dB)	87.7	74.0
DR	20kHzLPF + A-weighted	90.9	76.8
S/N	20kHzLPF + A-weighted	93.0	77.0

6. DAC (MOUT2) characteristics (R_L=10kΩ, DAC → MIX → MOUT2)

		[dB]
THD+N	20kHzLPF (-3dB)	87.9
DR	20kHzLPF + A-weighted	90.7
S/N	20kHzLPF + A-weighted	92.7

2. 16bit Mono CODEC

[Measurement condition]

- Measurement unit : ROHDE & SCHWARZ, UPD05
- BBICK : 32fs
- fs : 8kHz
- Bit : 16bit
- Power Supply : AVDD=BVDD=DVDD=3.3V
- Measurement Filter : 20Hz ~ 4kHz
- Temperature : Room

[Measurement Results]

1. ADC (AUXIN) characteristics (MICAD =0, AUXIN → Mixer → ADC, AUX Volume = 0dB)

		[dB]
THD+N	20kHzLPF (-1dB)	78.5
DR	20kHzLPF + A-weighted	88.7
S/N	20kHzLPF + A-weighted	88.9

2. DAC (MOUT) characteristics (R_L=20kΩ, DAC → MOUT, ATT = 0dB)

		[dB]
THD+N	20kHzLPF (-0dB)	78.9
DR	20kHzLPF + A-weighted	91.4
S/N	20kHzLPF + A-weighted	92.0

3. Loop-back (AUXIN → ADC → DAC → MOUT)

		[dB]
THD+N	20kHzLPF (-3dB)	76.7
DR	20kHzLPF + A-weighted	87.9
S/N	20kHzLPF + A-weighted	88.0

3. 16bit stereo CODEC PLOT DATA
3-1. ADC (MIC → IPGA → ADC) PLOT DATA

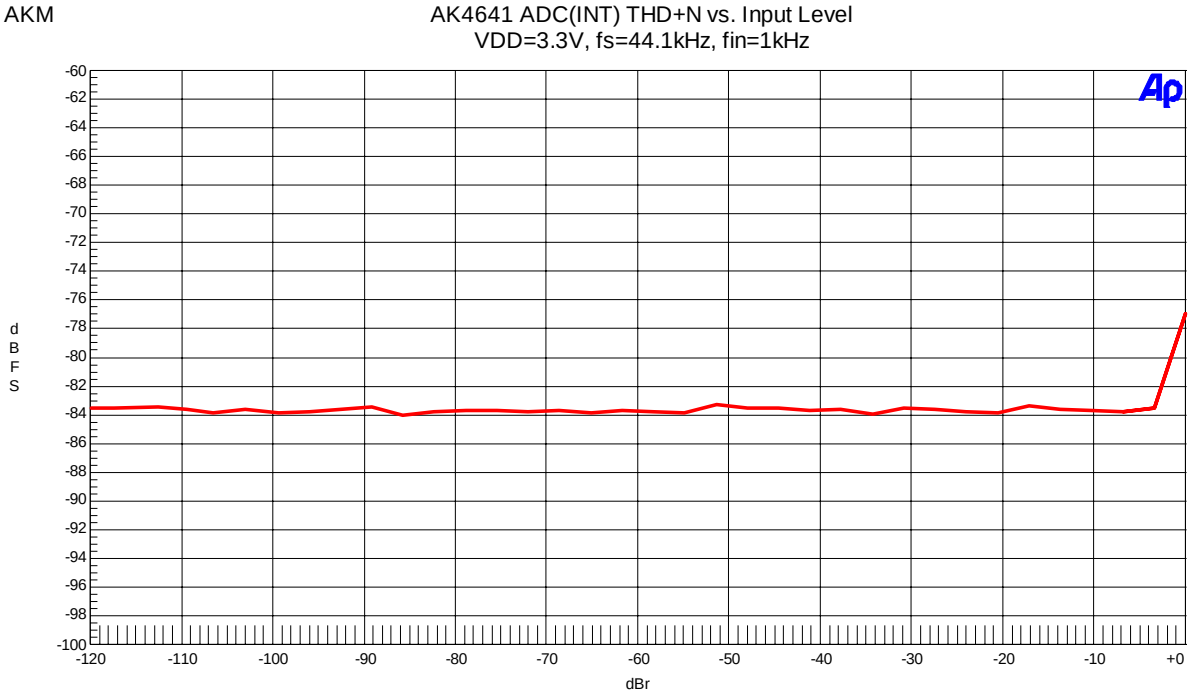


Figure 1. THD+N vs. Input Level

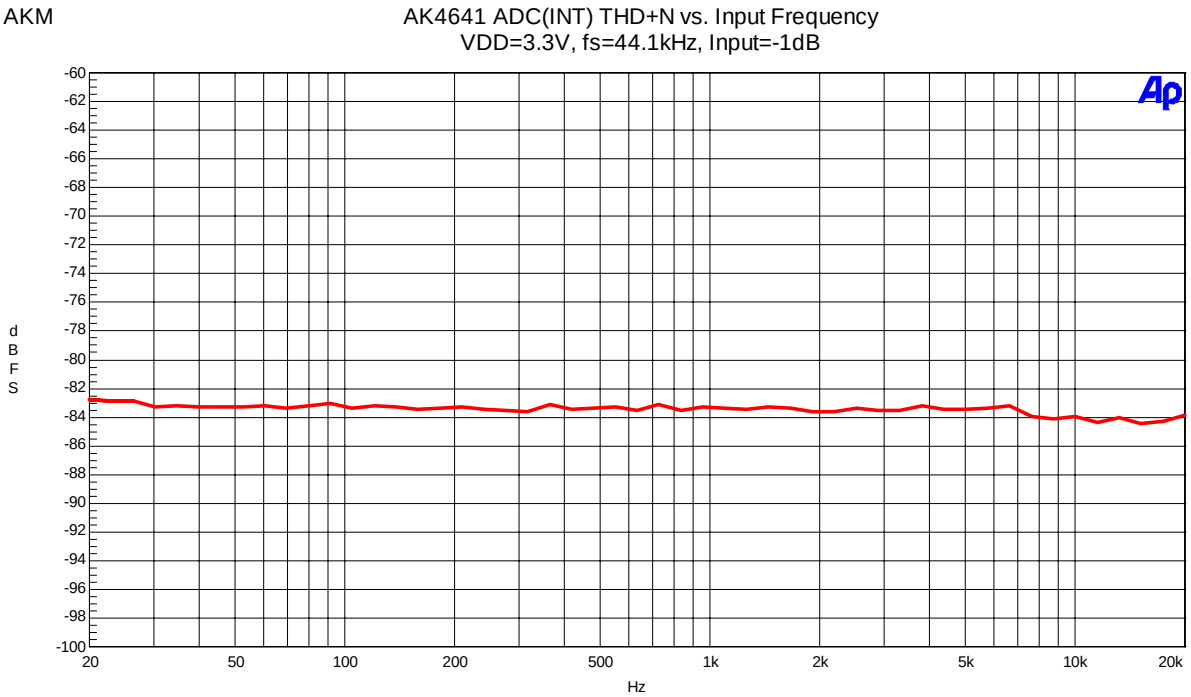


Figure 2. THD+N vs. Input Frequency

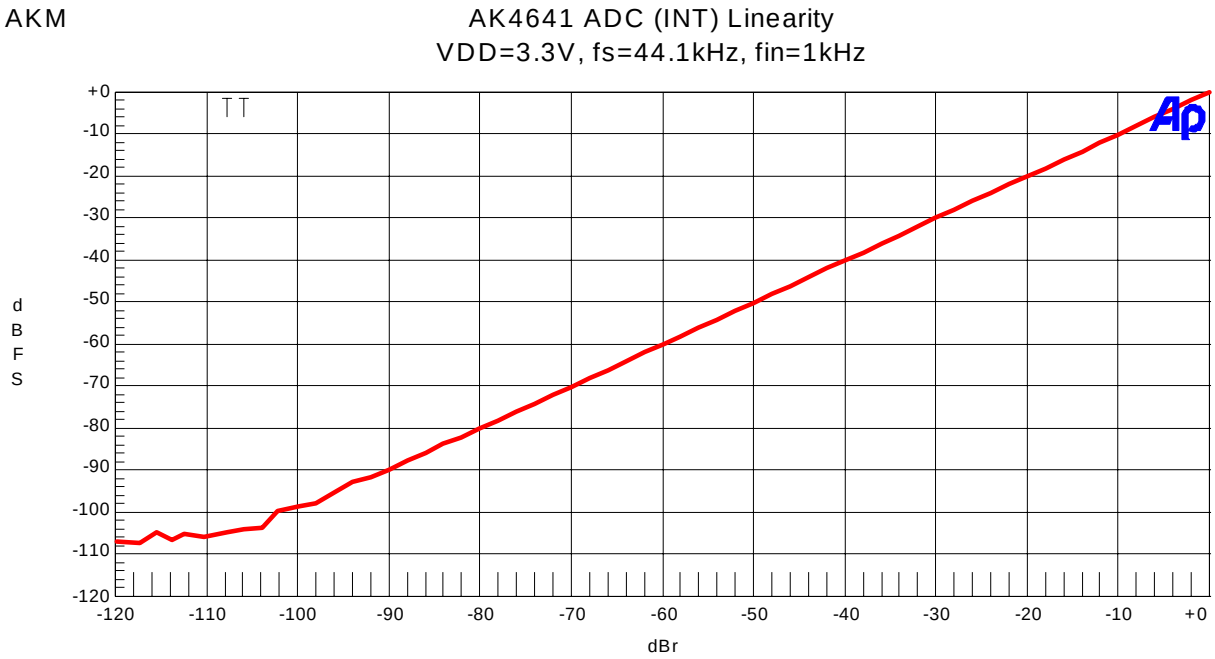


Figure 3. Linearity

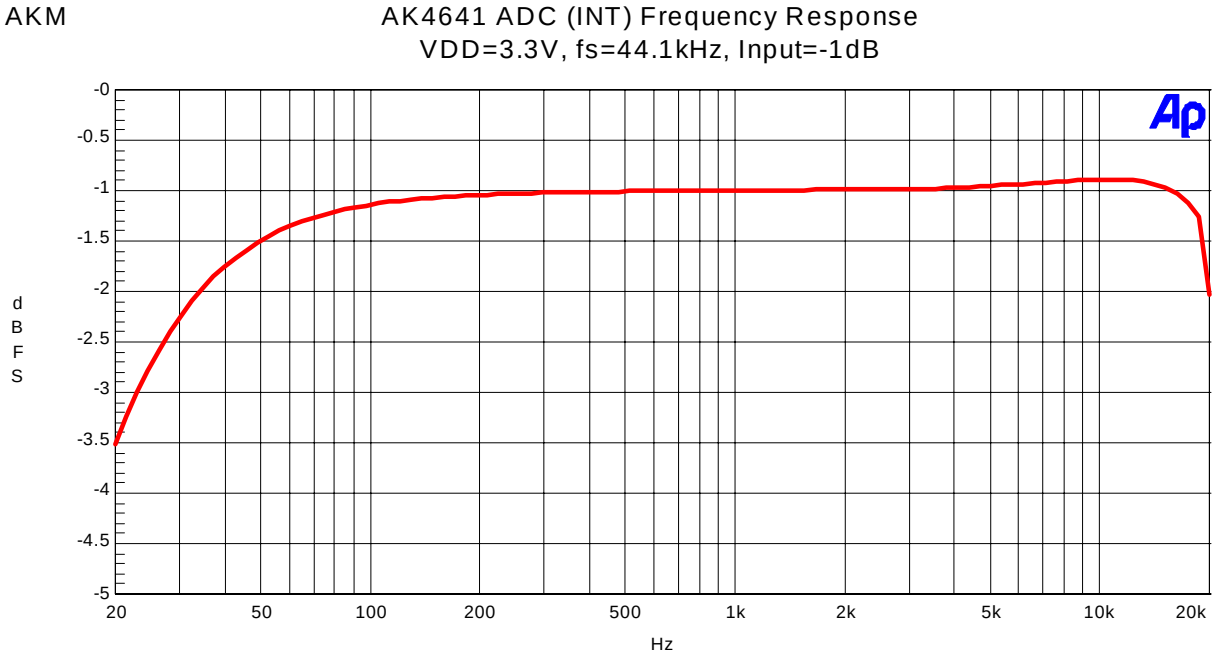


Figure 4. Frequency Response

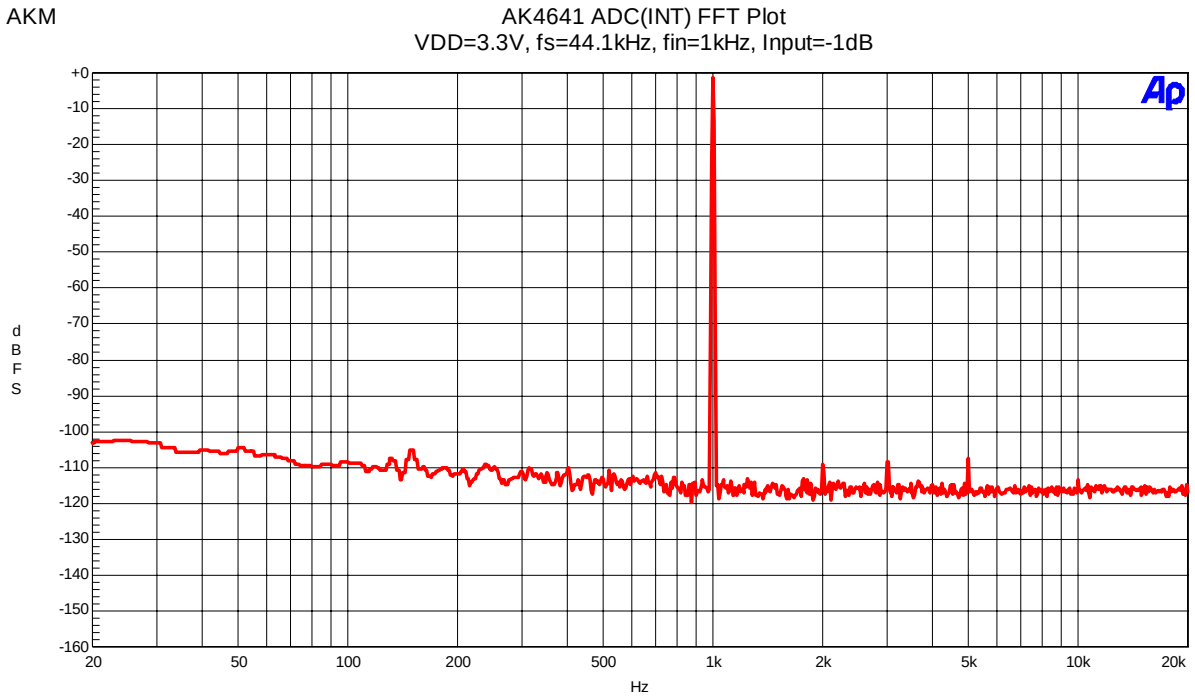


Figure 5. FFT Plot (Input level=-1dBFS)

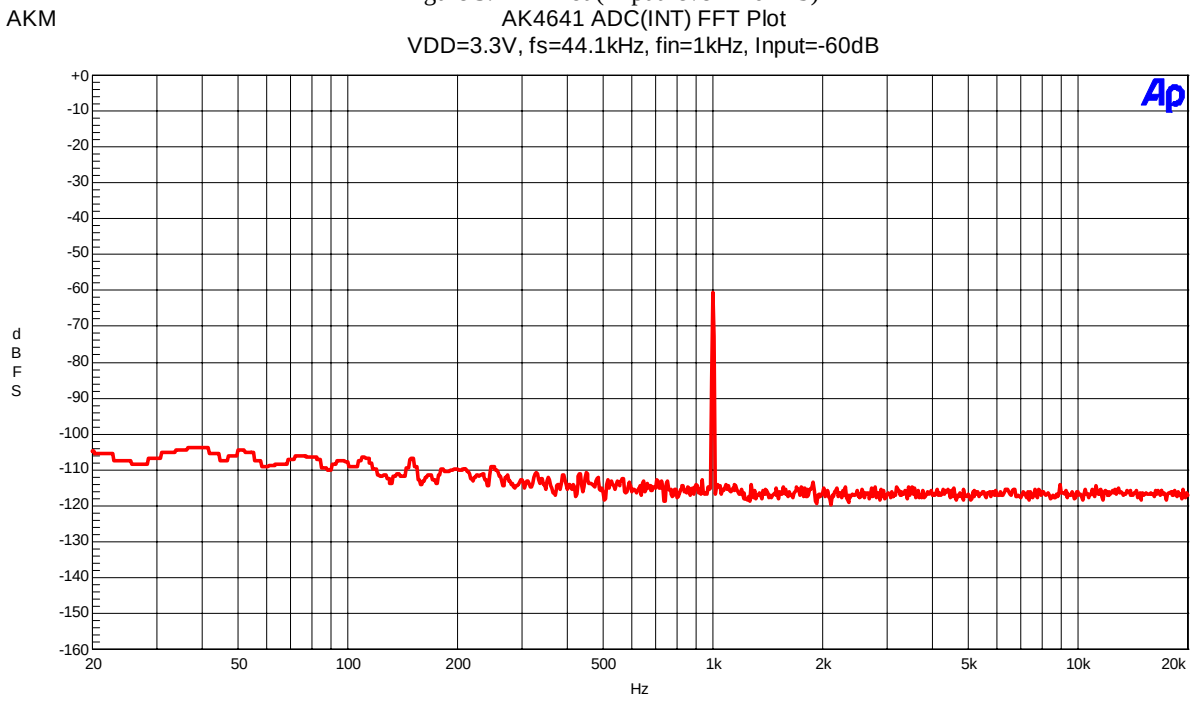


Figure 6. FFT Plot (Input level=-60dBFS)

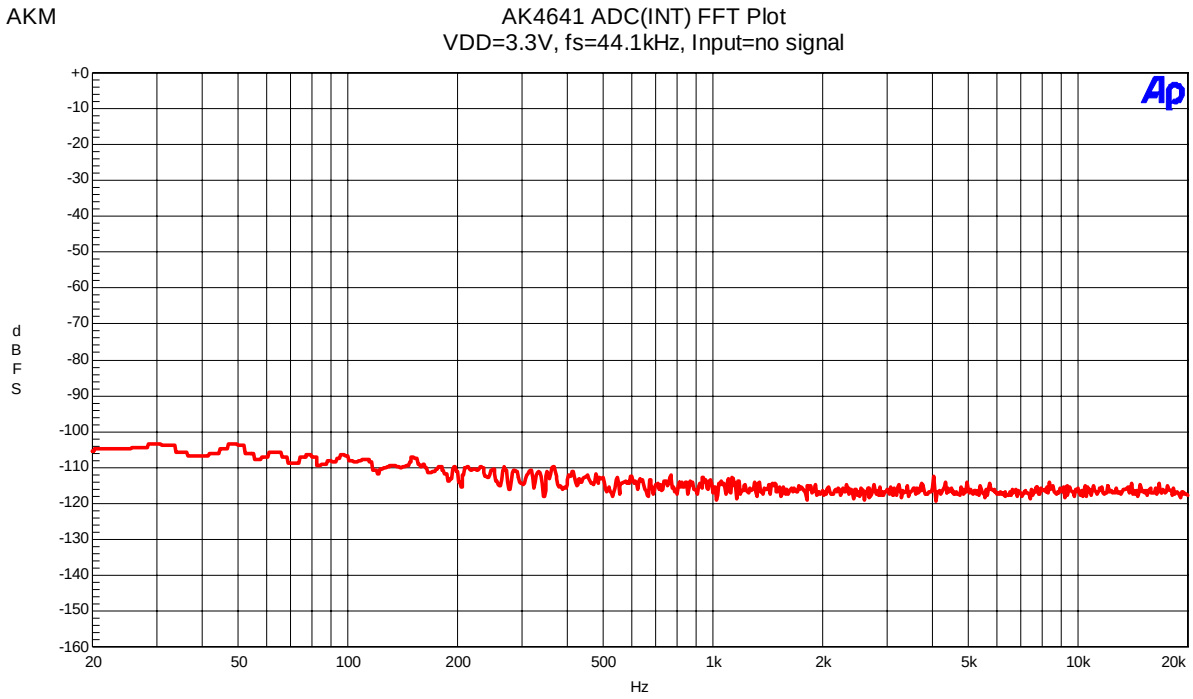


Figure 7. FFT Plot (No signal)

3-2. DAC (DAC → Mono Out) PLOT DATA

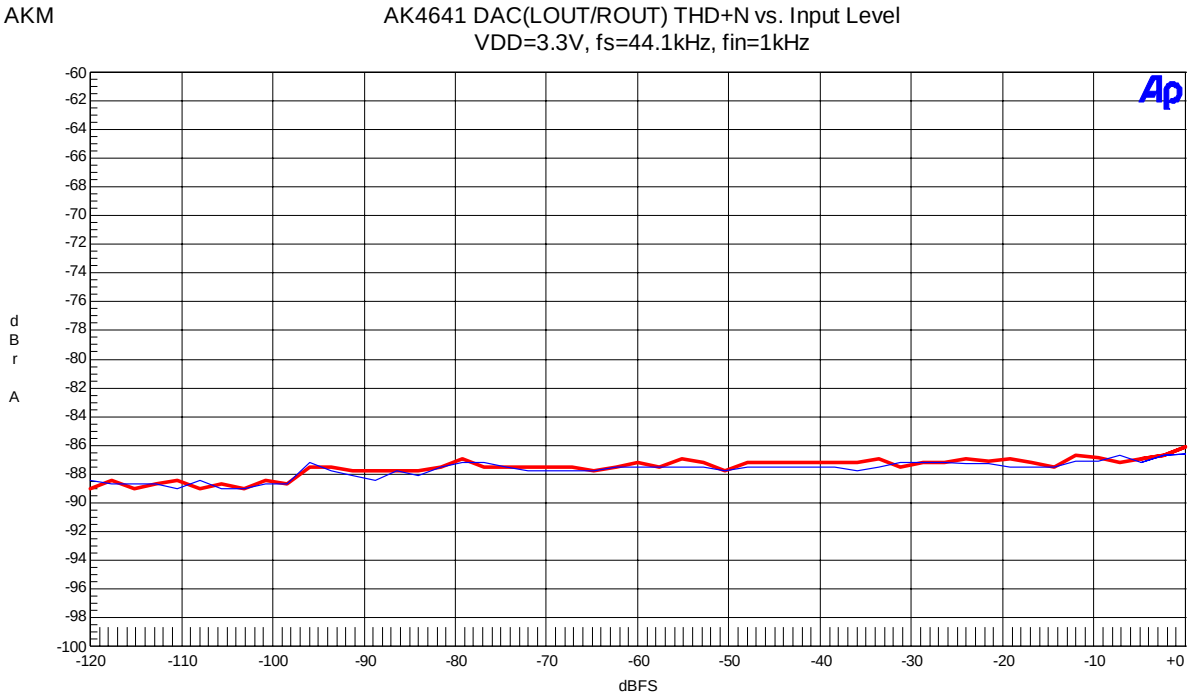


Figure 8. THD+N vs. Input Level

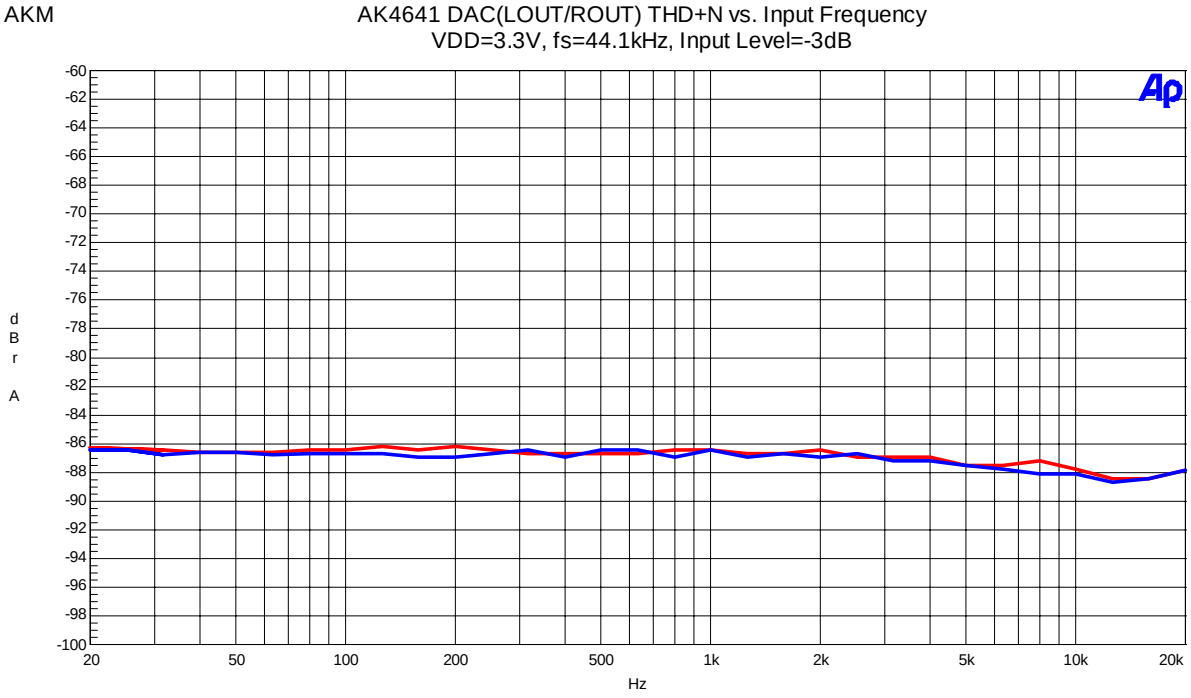


Figure 9. THD+N vs. Input Frequency

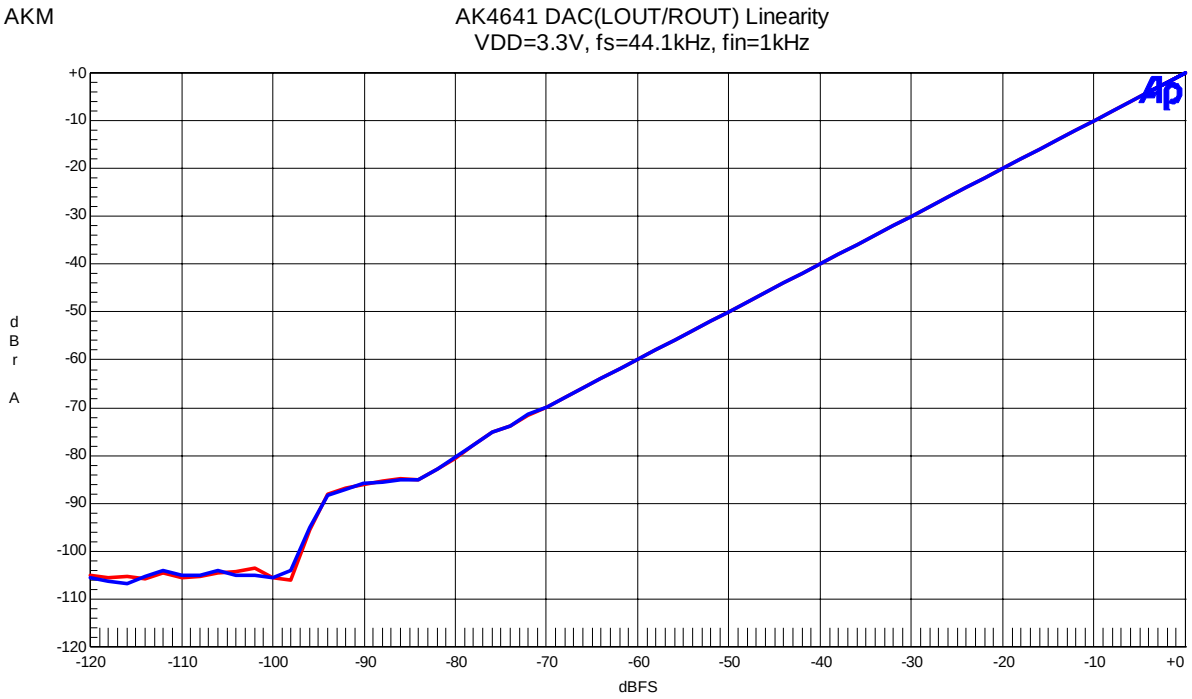


Figure 10 Linearity

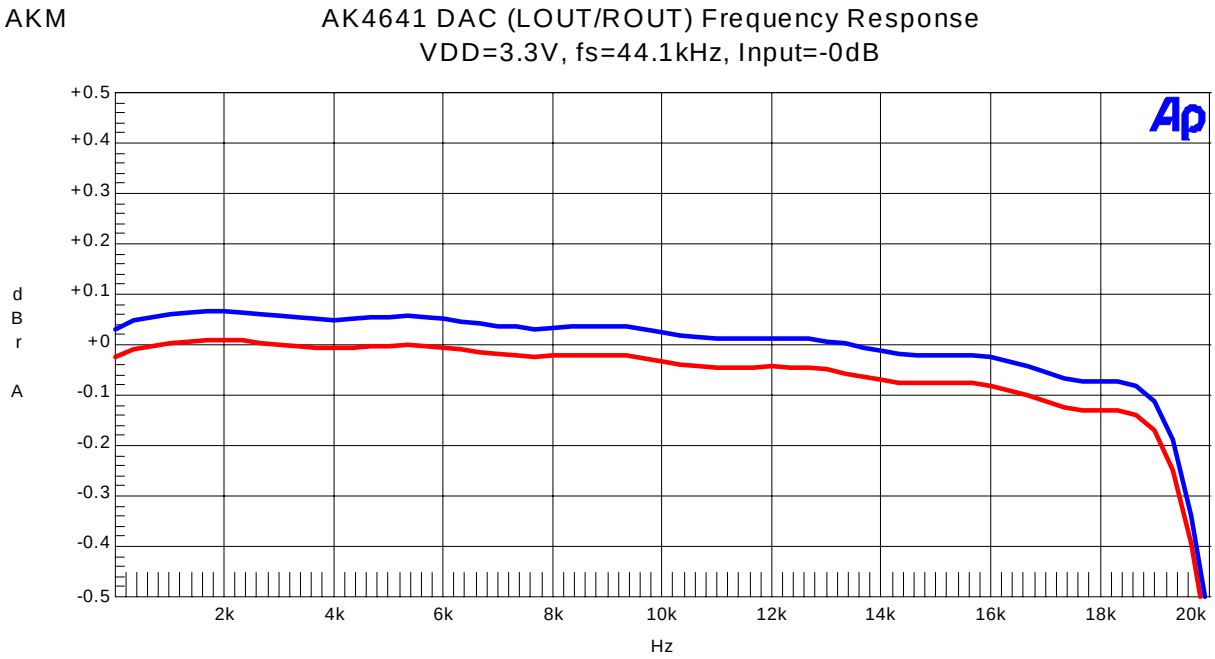


Figure 11. Frequency Response

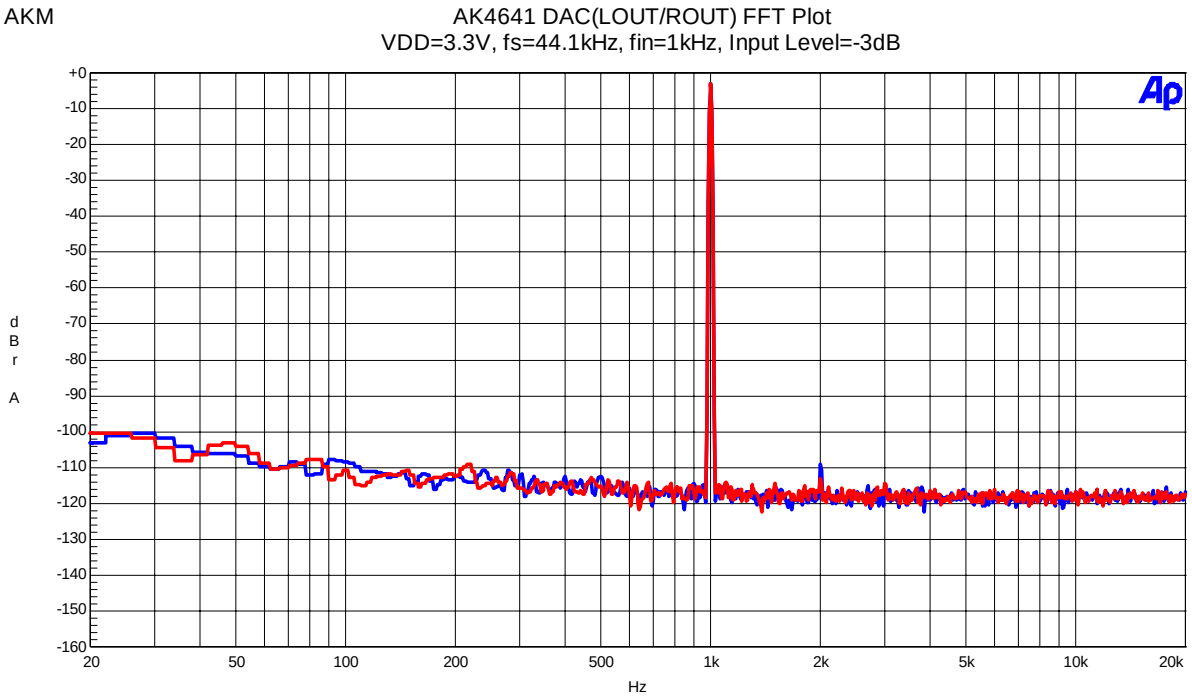


Figure 12. FFT Plot (Input level=-3dBFS)

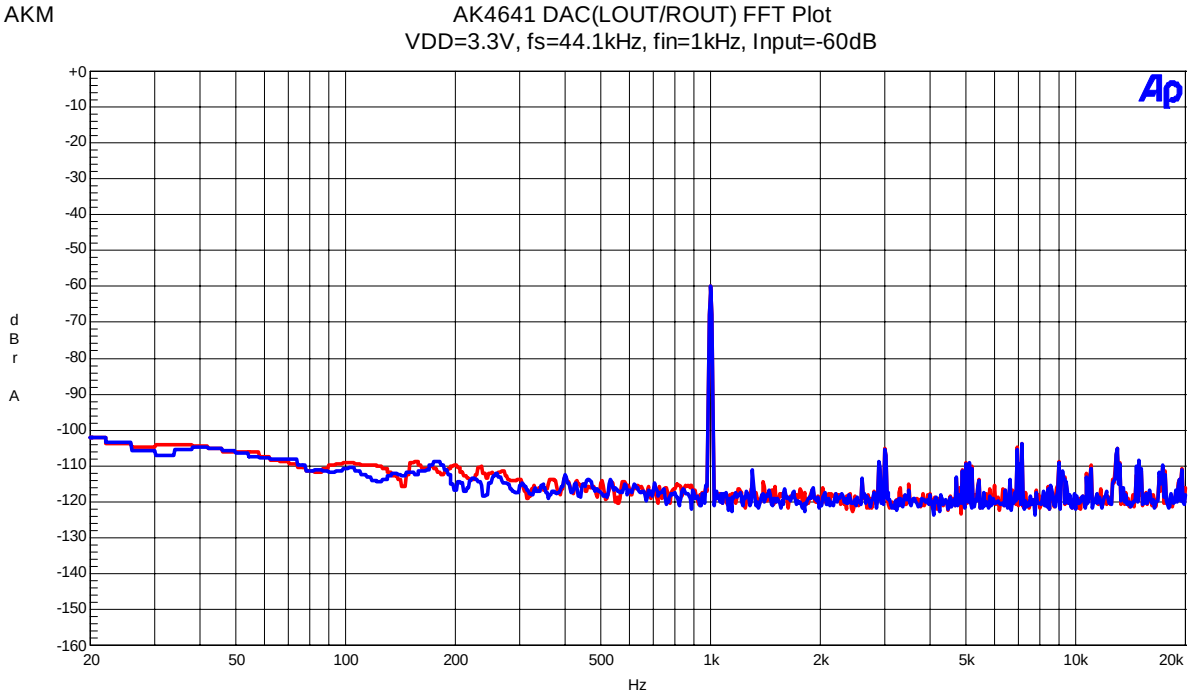


Figure 13. FFT Plot (Input level=-60.0dBFS)

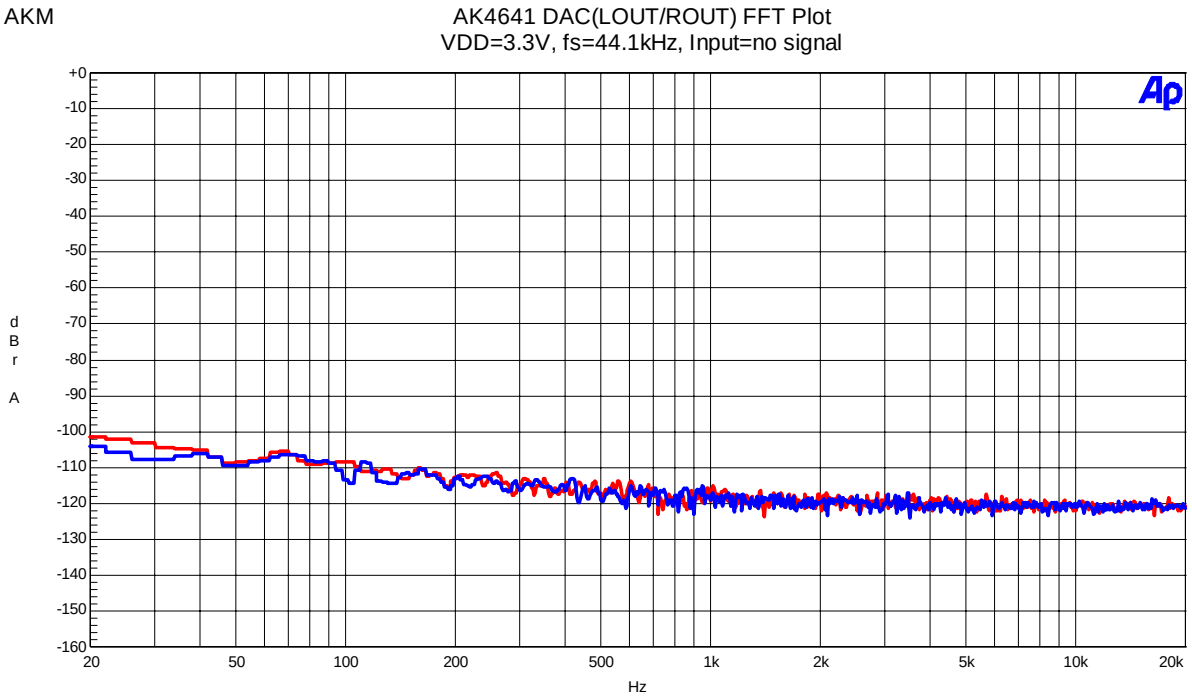


Figure 14. FFT Plot (No signal)

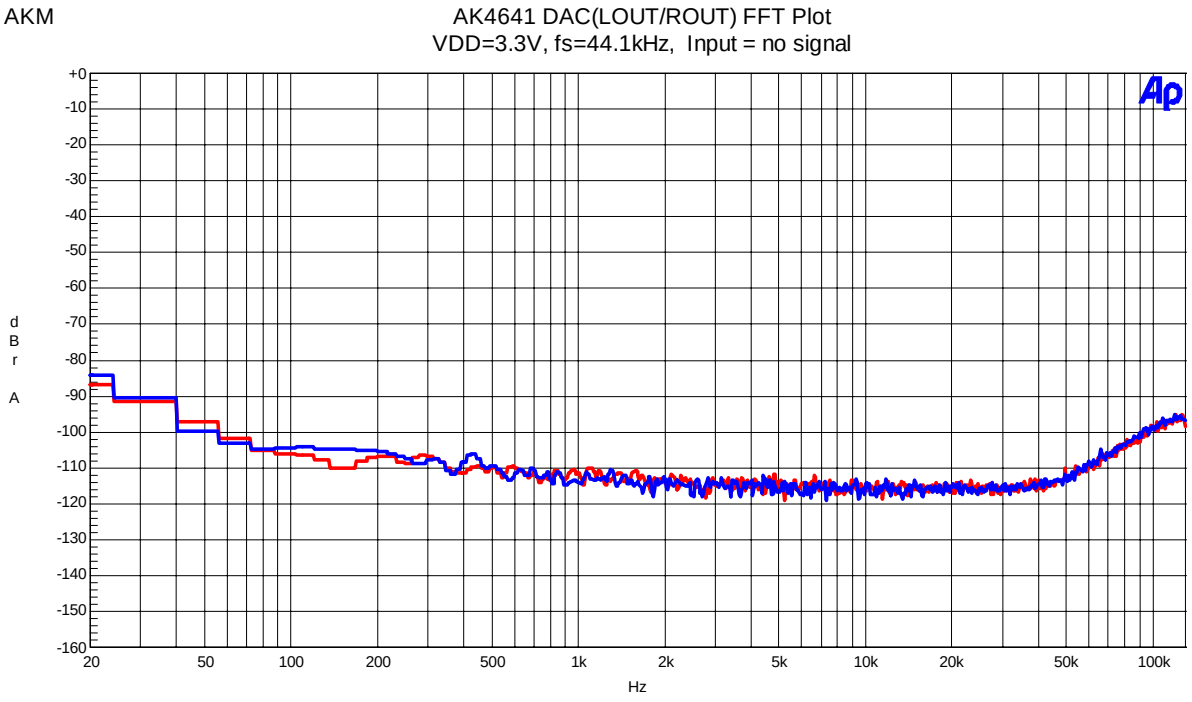


Figure 15. Out-of-band Noise

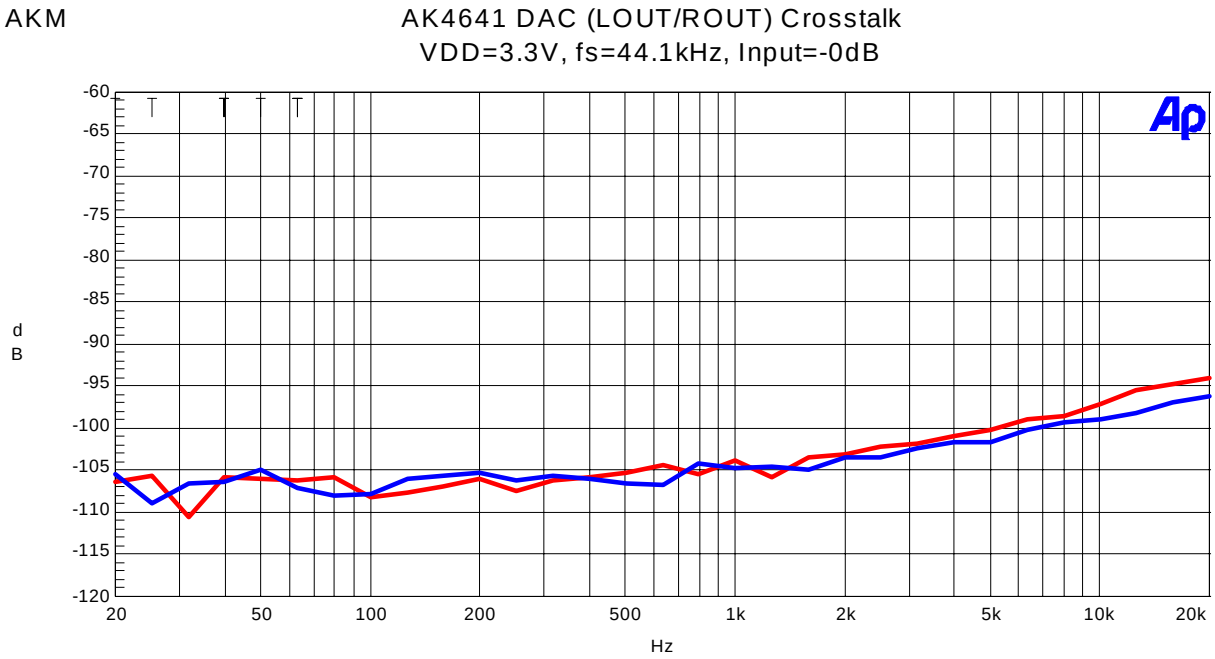


Figure 16. Crosstalk Plot

4. 16bit Mono CODEC PLOT DATA

4-1. ADC (AUXIN → Mixer → ADC) PLOT DATA

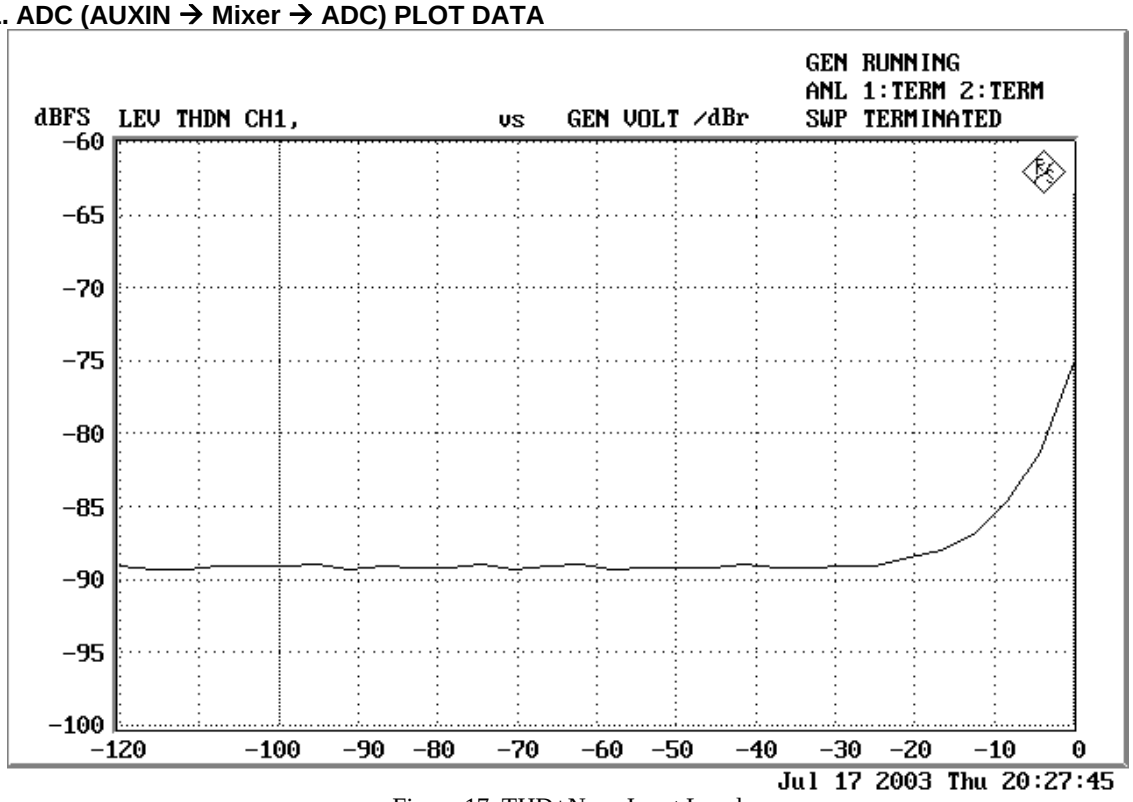


Figure 17. THD+N vs. Input Level

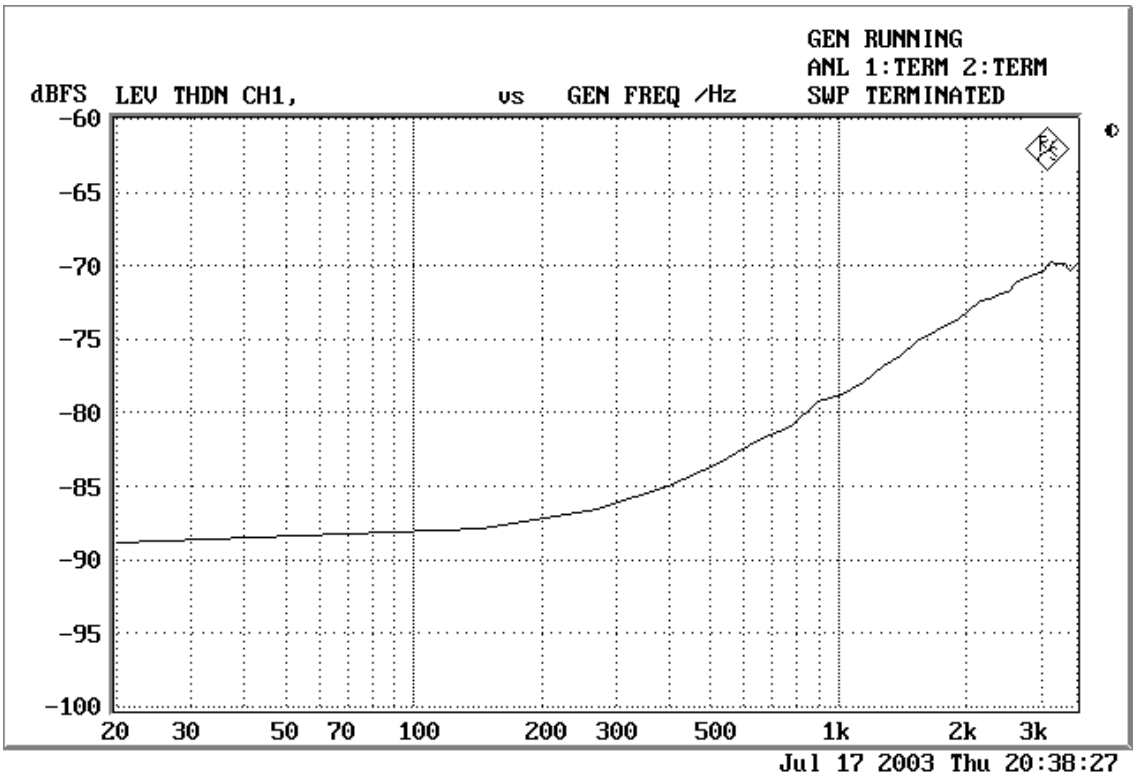


Figure 18. THD+N vs. Input Frequency

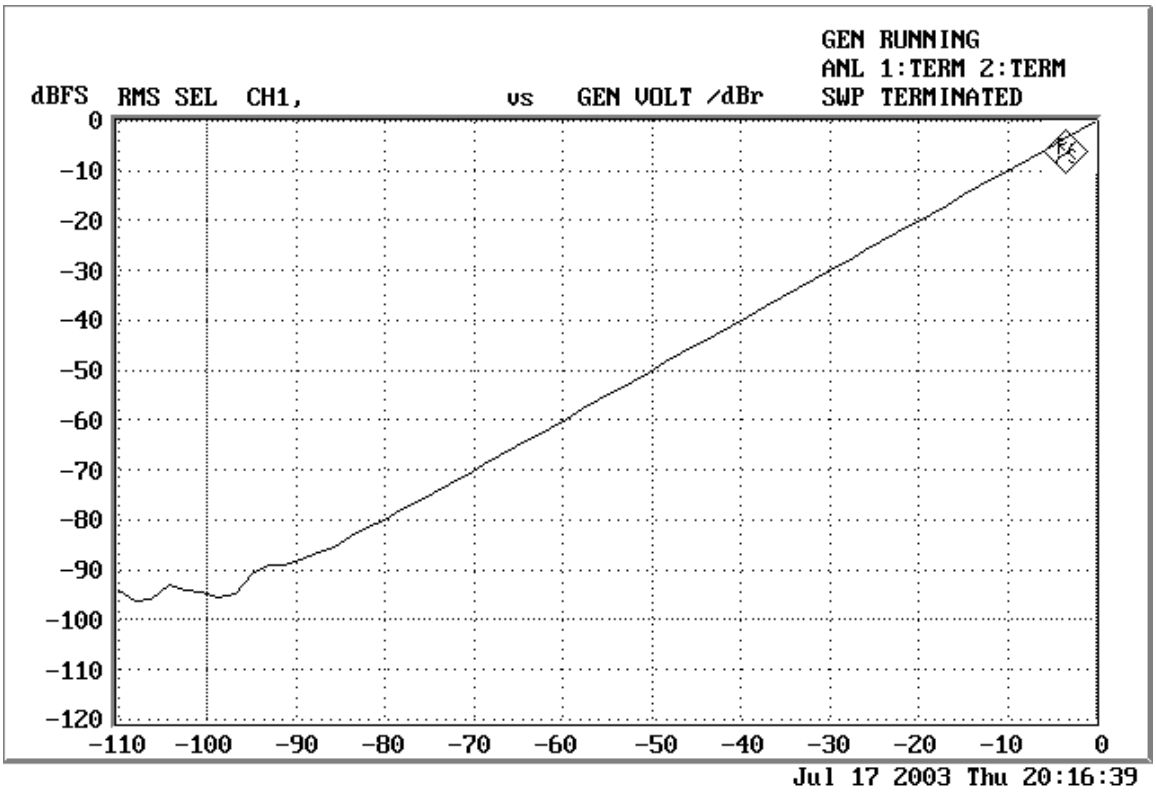


Figure 19. Linearity

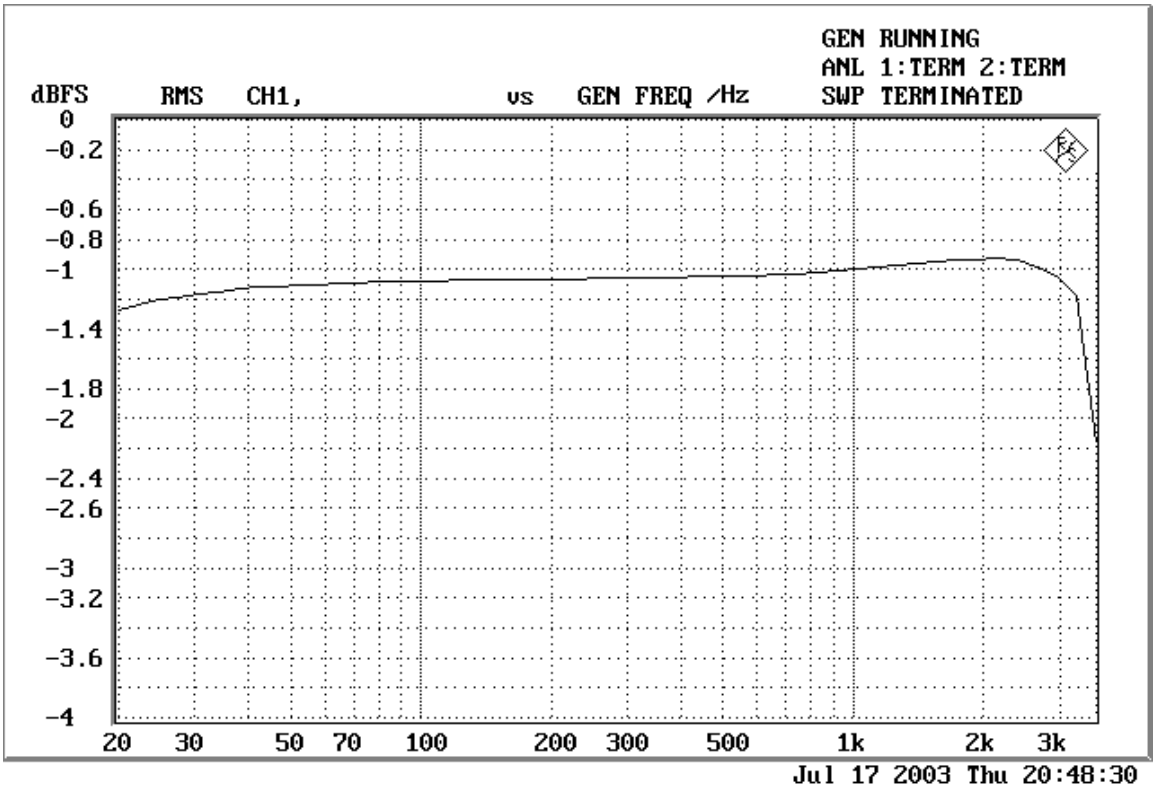


Figure 20. Frequency Response

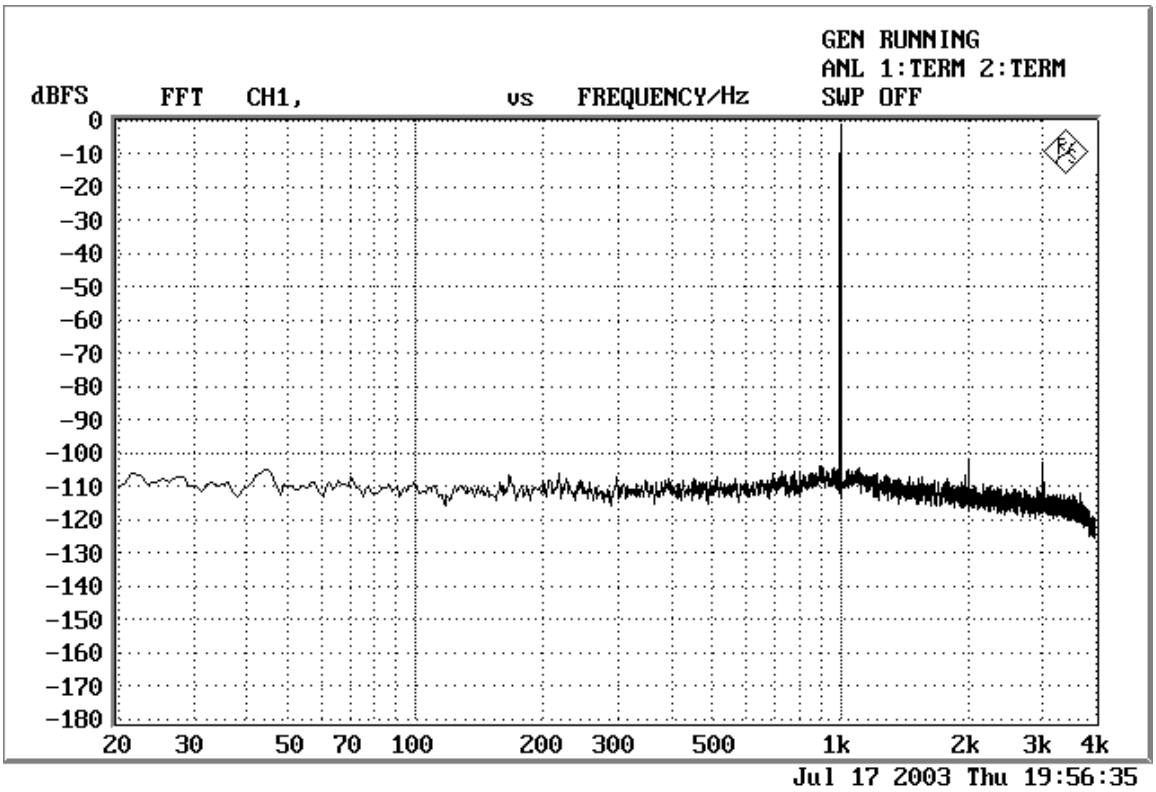


Figure 21. FFT Plot (Input level=-1dBFS)

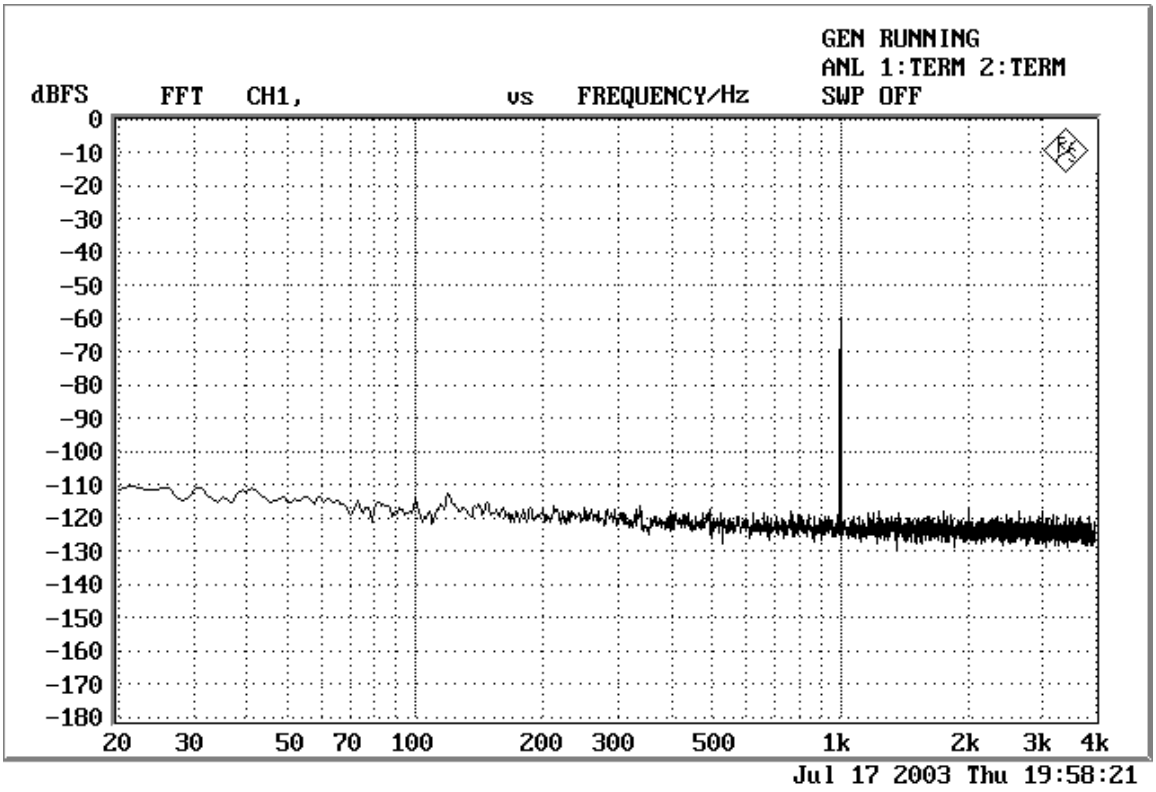


Figure 22. FFT Plot (Input level=-60dBFS)

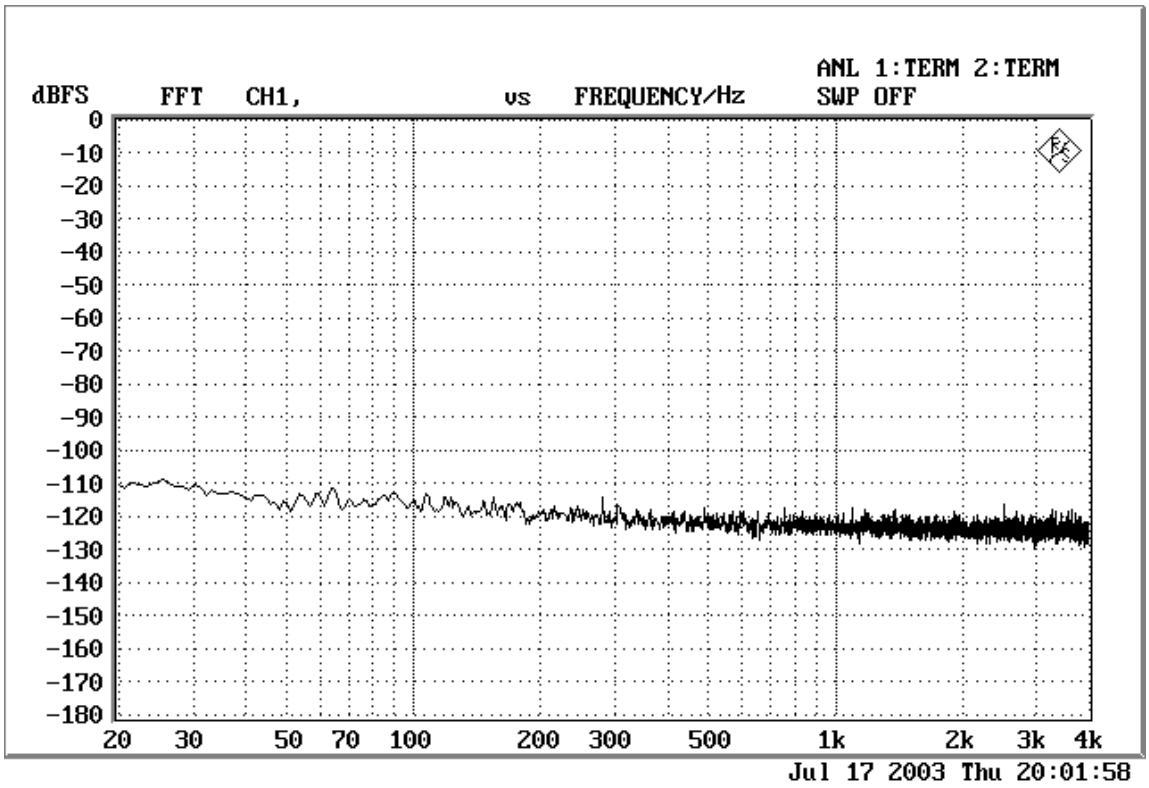


Figure 23. FFT Plot (No signal)

4-2. DAC (DAC → Mono Out) PLOT DATA

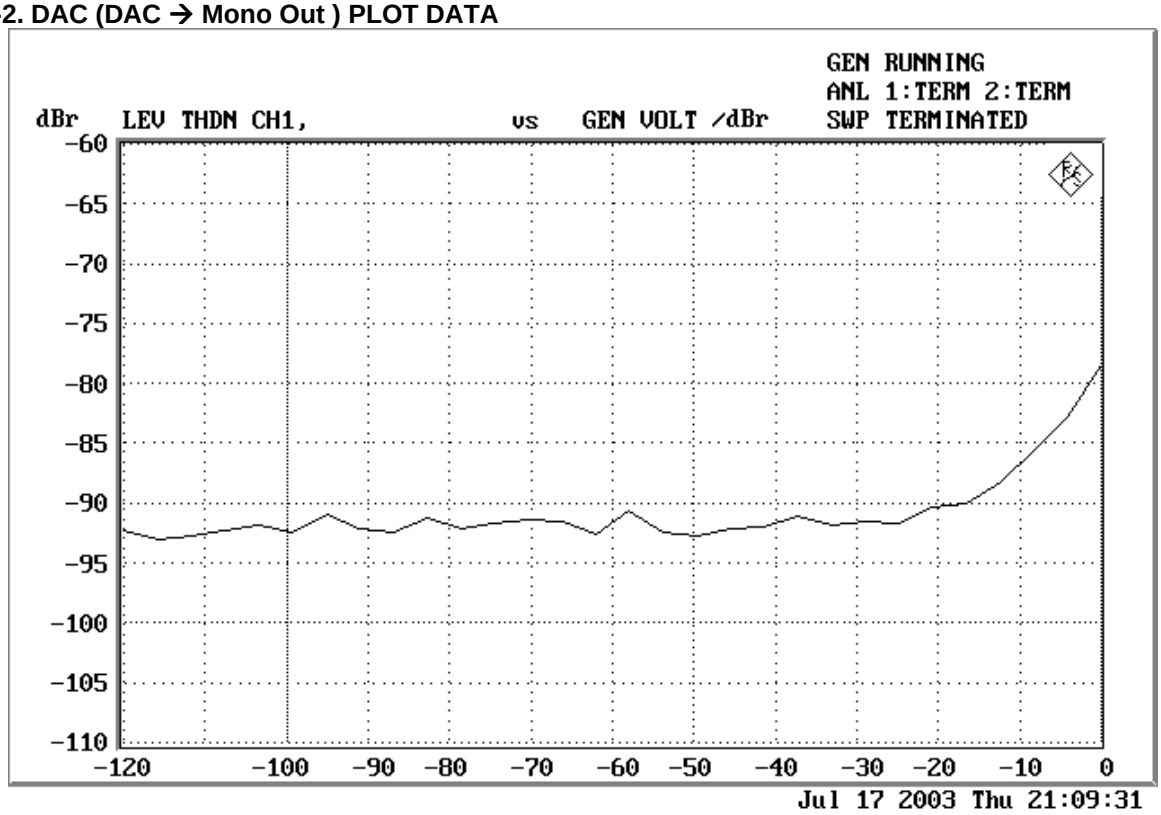


Figure 24. THD+N vs. Input Level

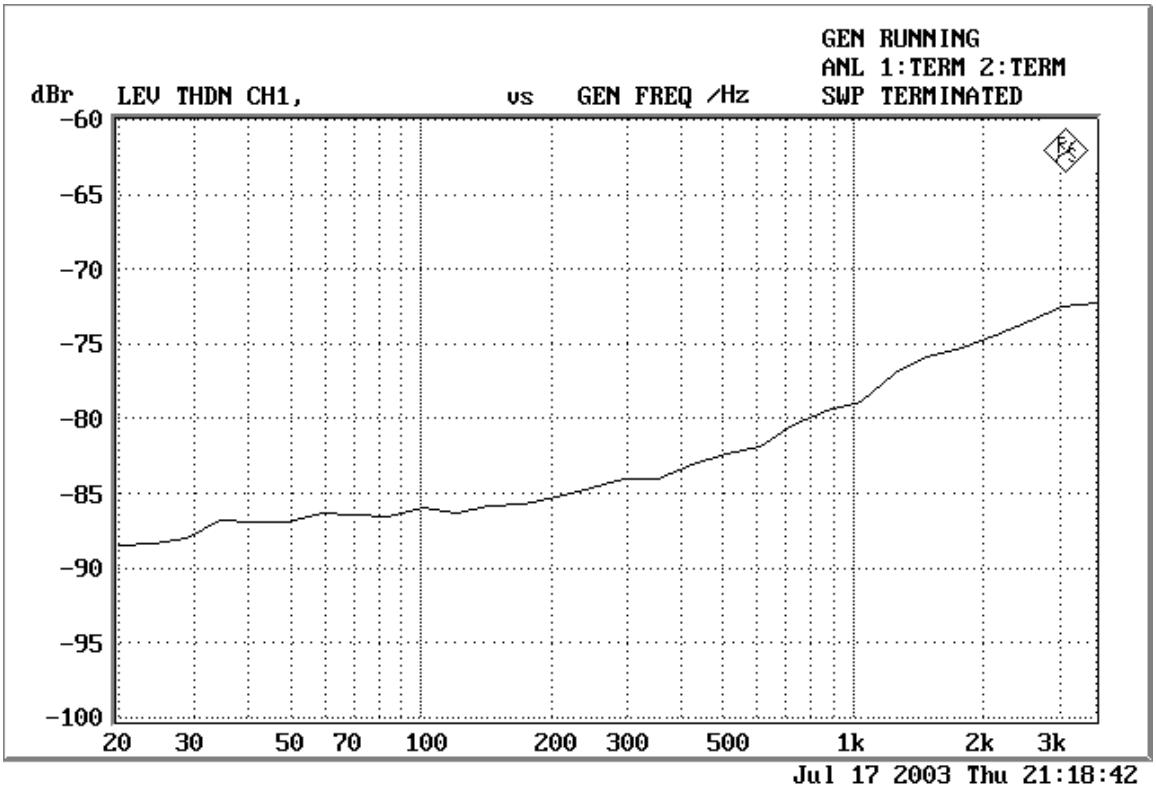


Figure 25. THD+N vs. Input Frequency

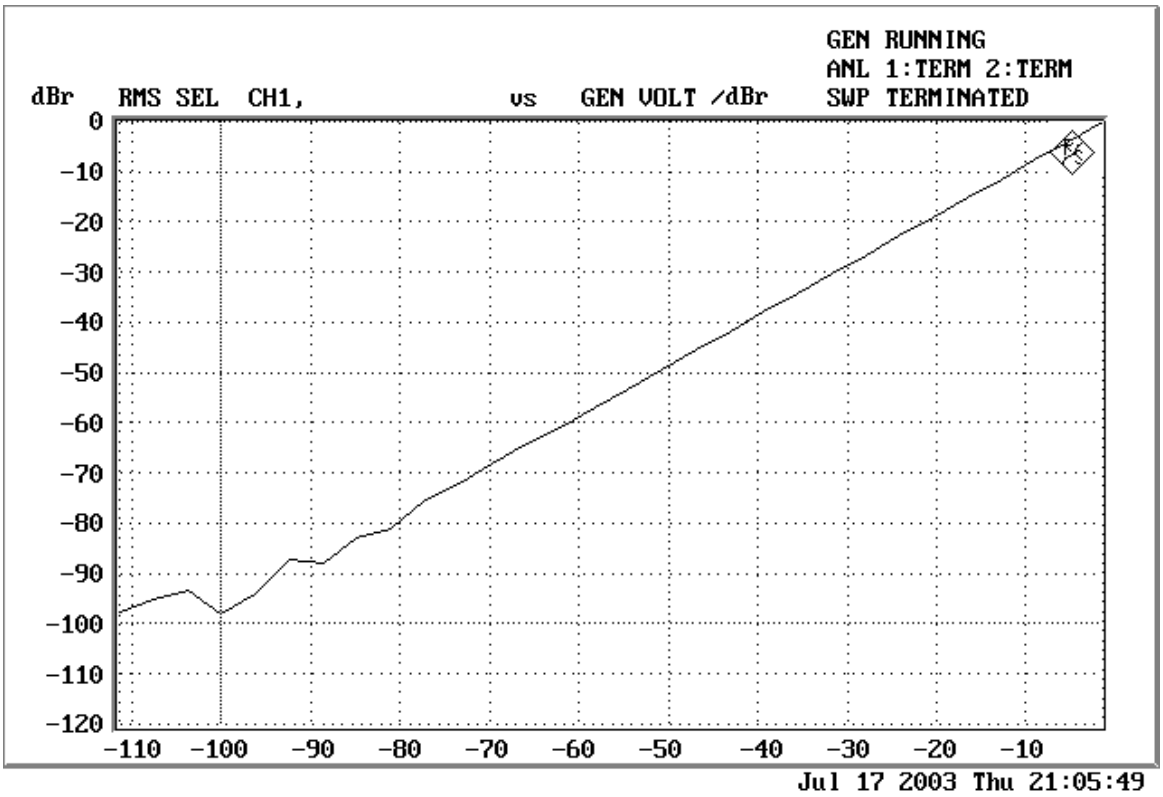


Figure 26 Linearity

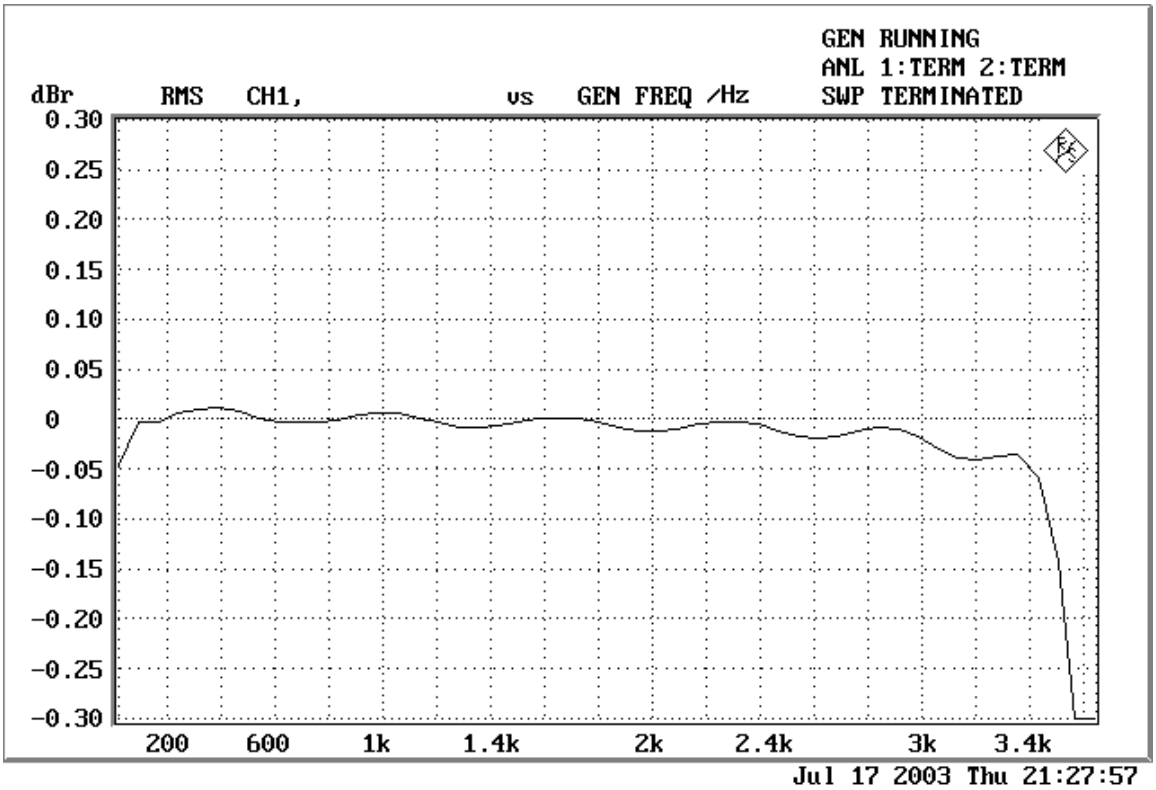


Figure 27. Frequency Response

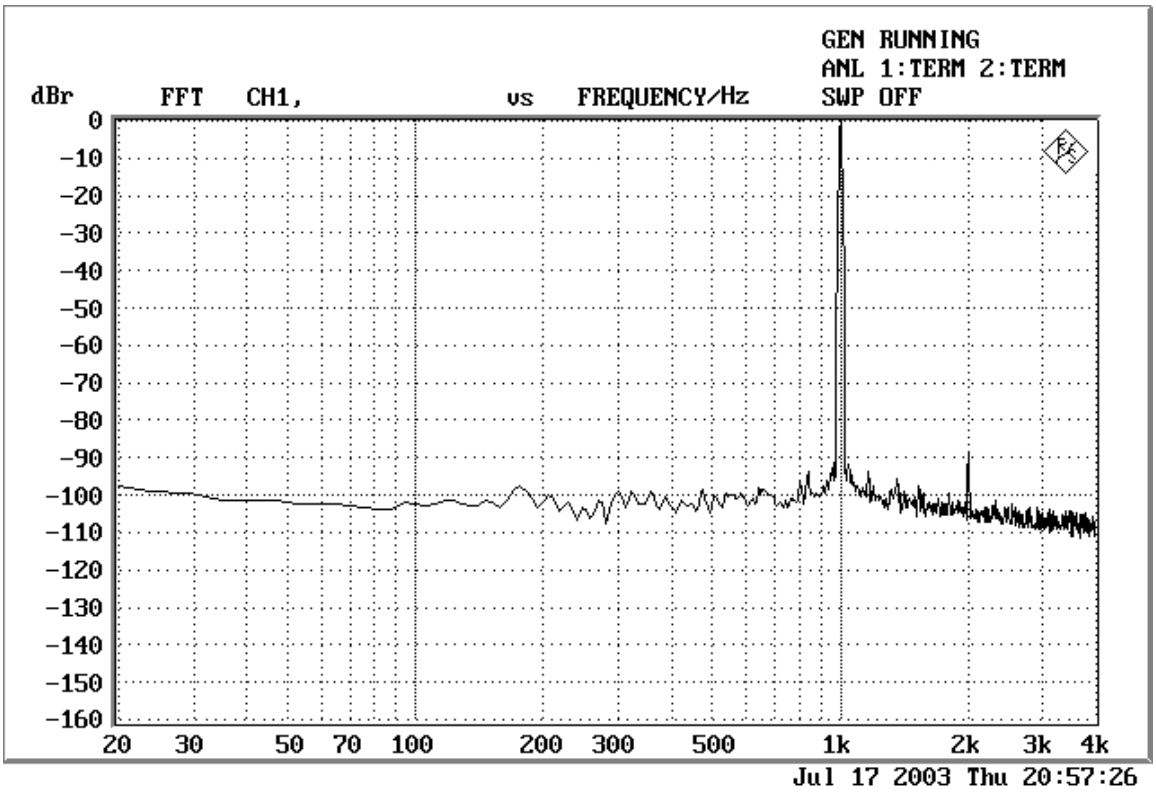


Figure 28. FFT Plot (Input level=-0dBFS)

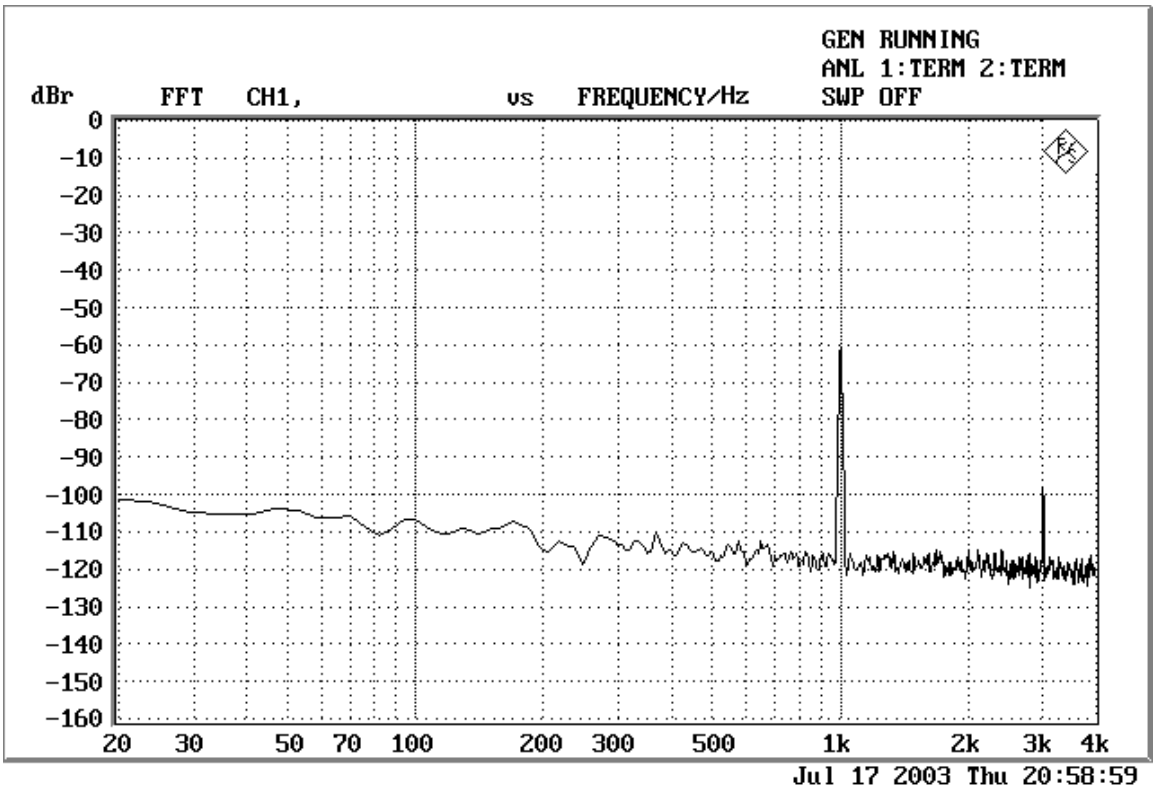


Figure 29. FFT Plot (Input level=-60.0dBFS)

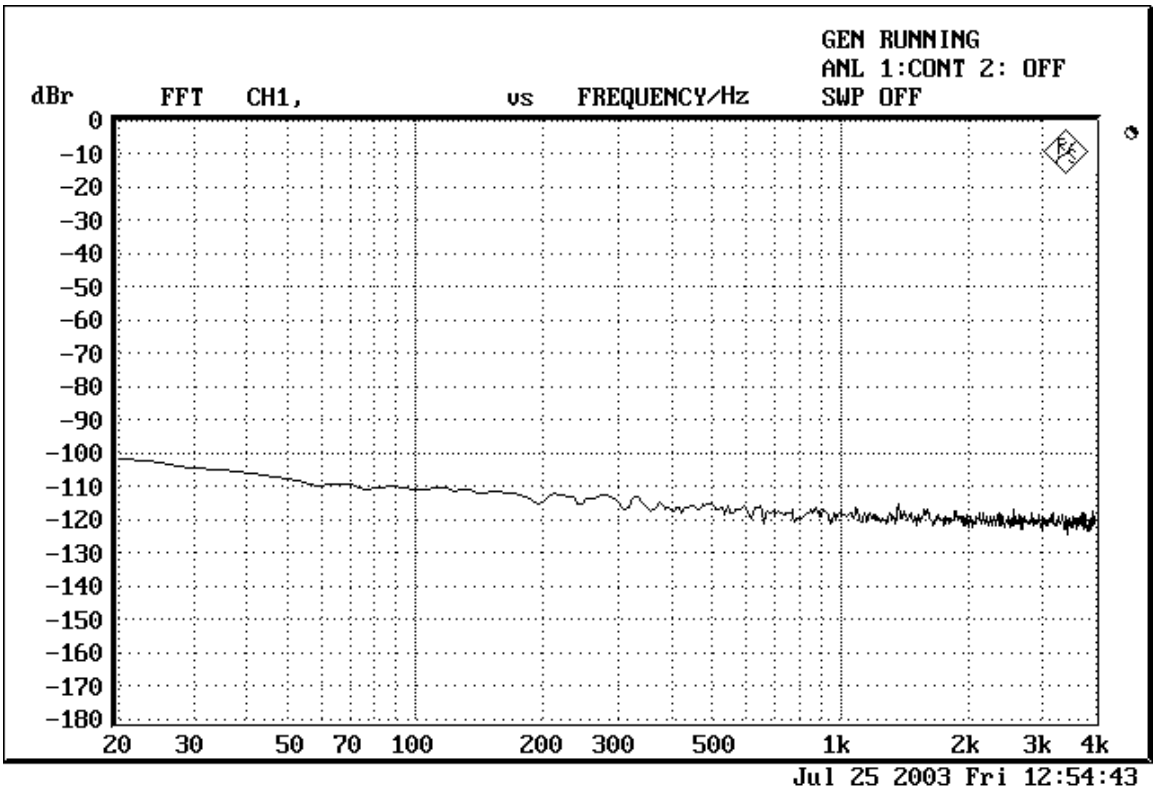
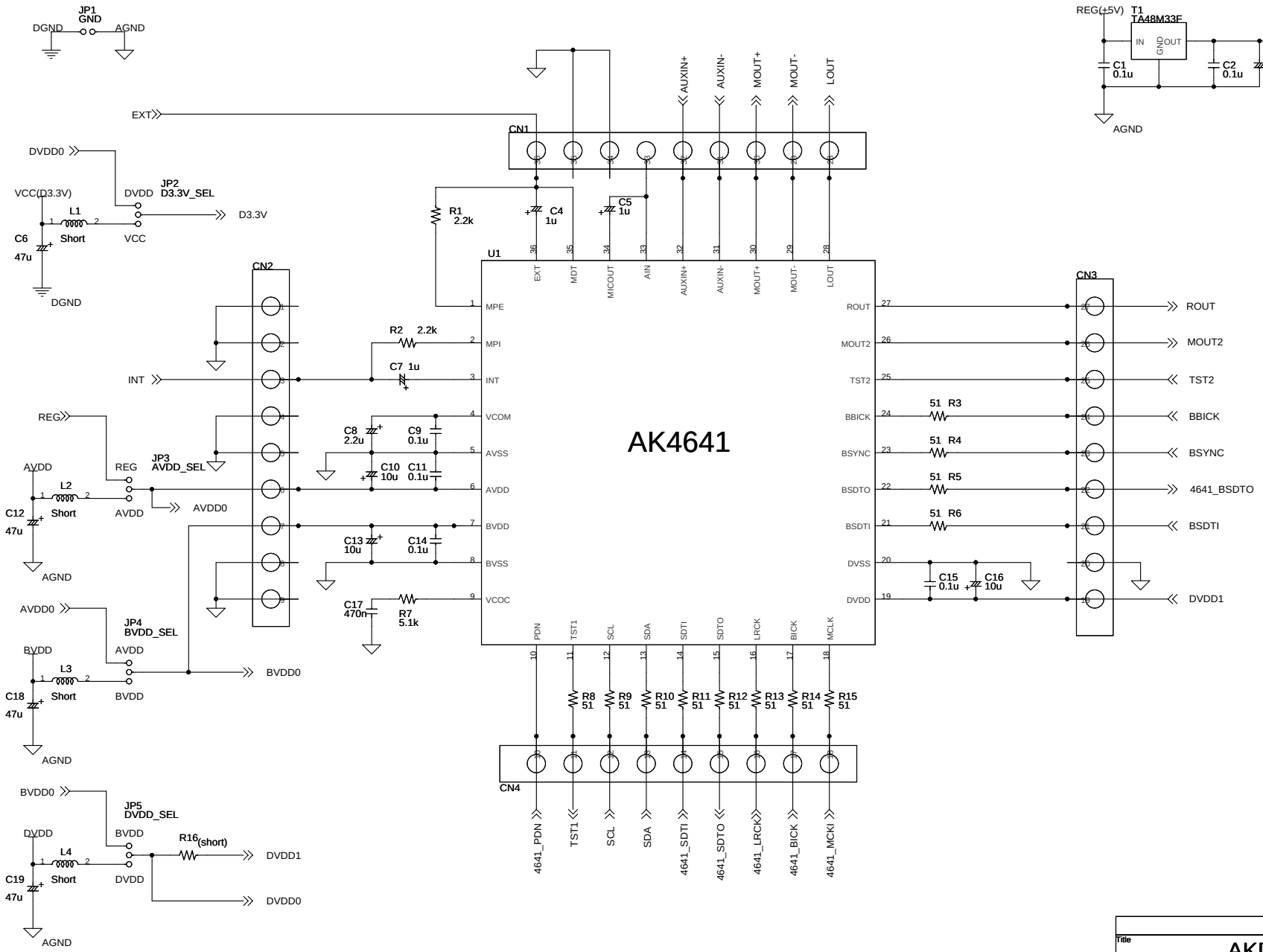


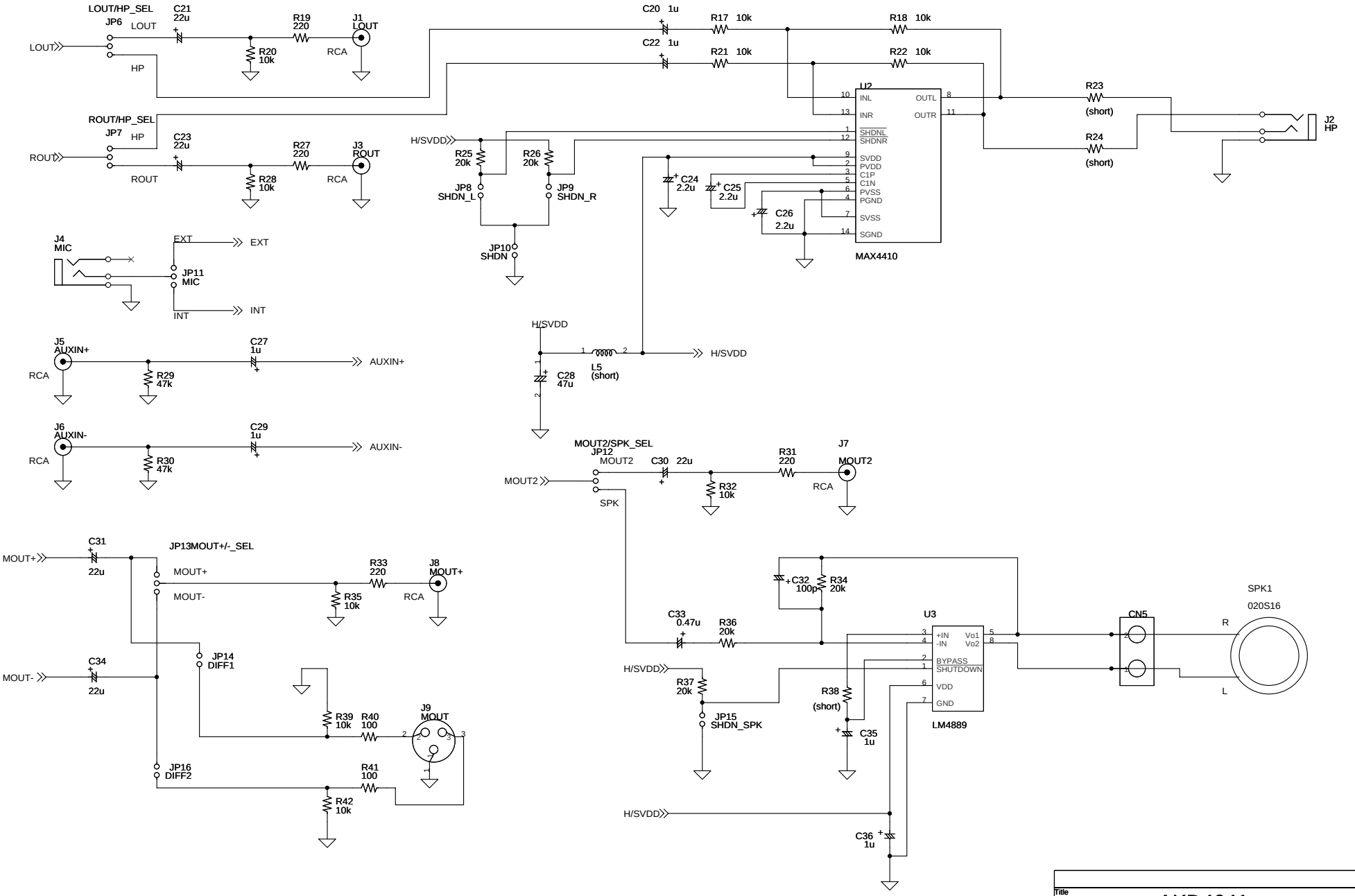
Figure 30. FFT Plot (No signal)

Revision History

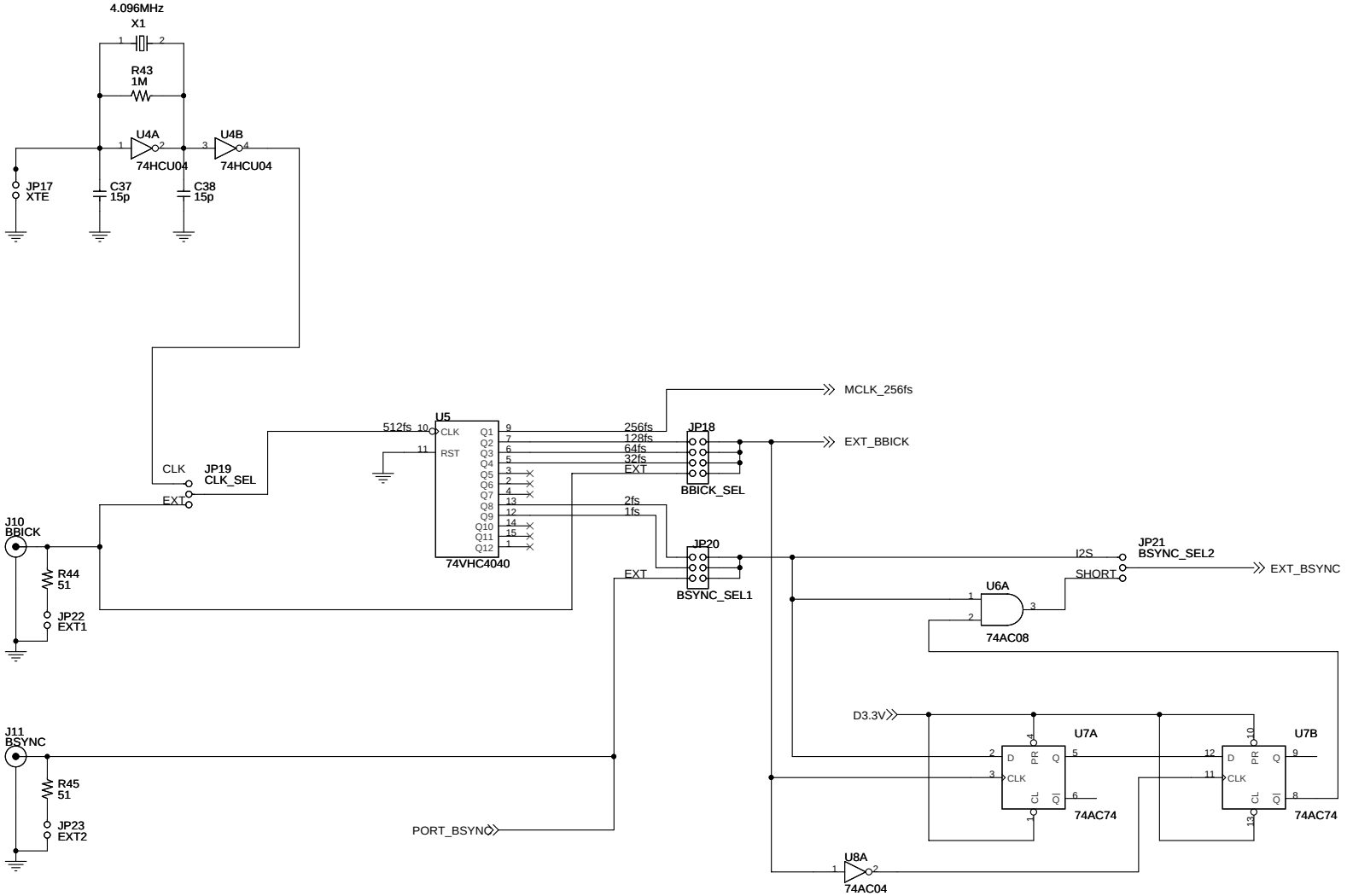
Date (YY/MM/DD)	Manual Revision	Board Revision	Reason	Contents
05/11/29	KM082000	0	First Edition	
06/03/13	KM082001	1	Update	Change of a figure & circuit



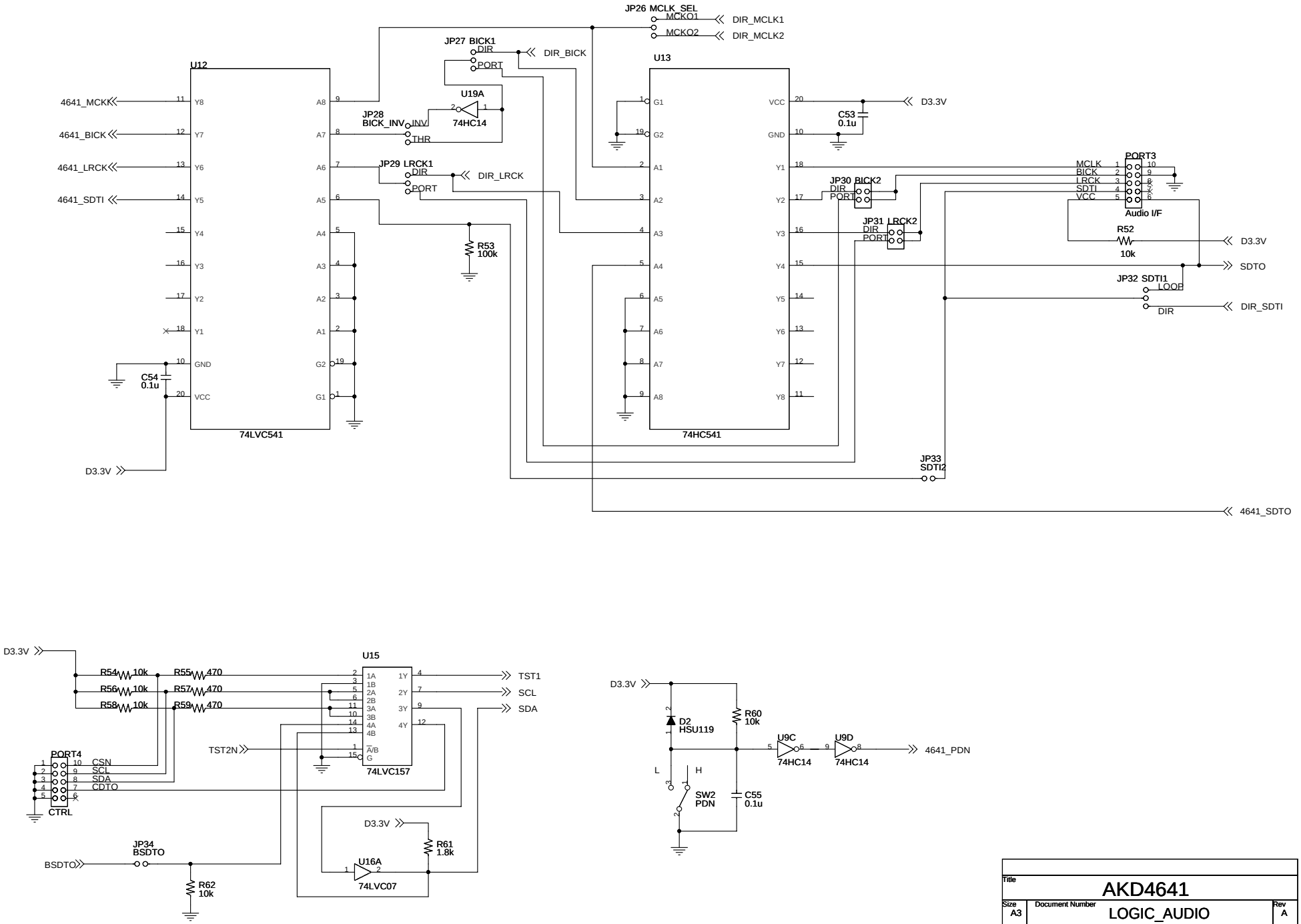
Title	AKD4641	
Size A3	Document Number AK4641	Rev A
Date: Friday, November 25, 2005	Sheet 1 of 6	



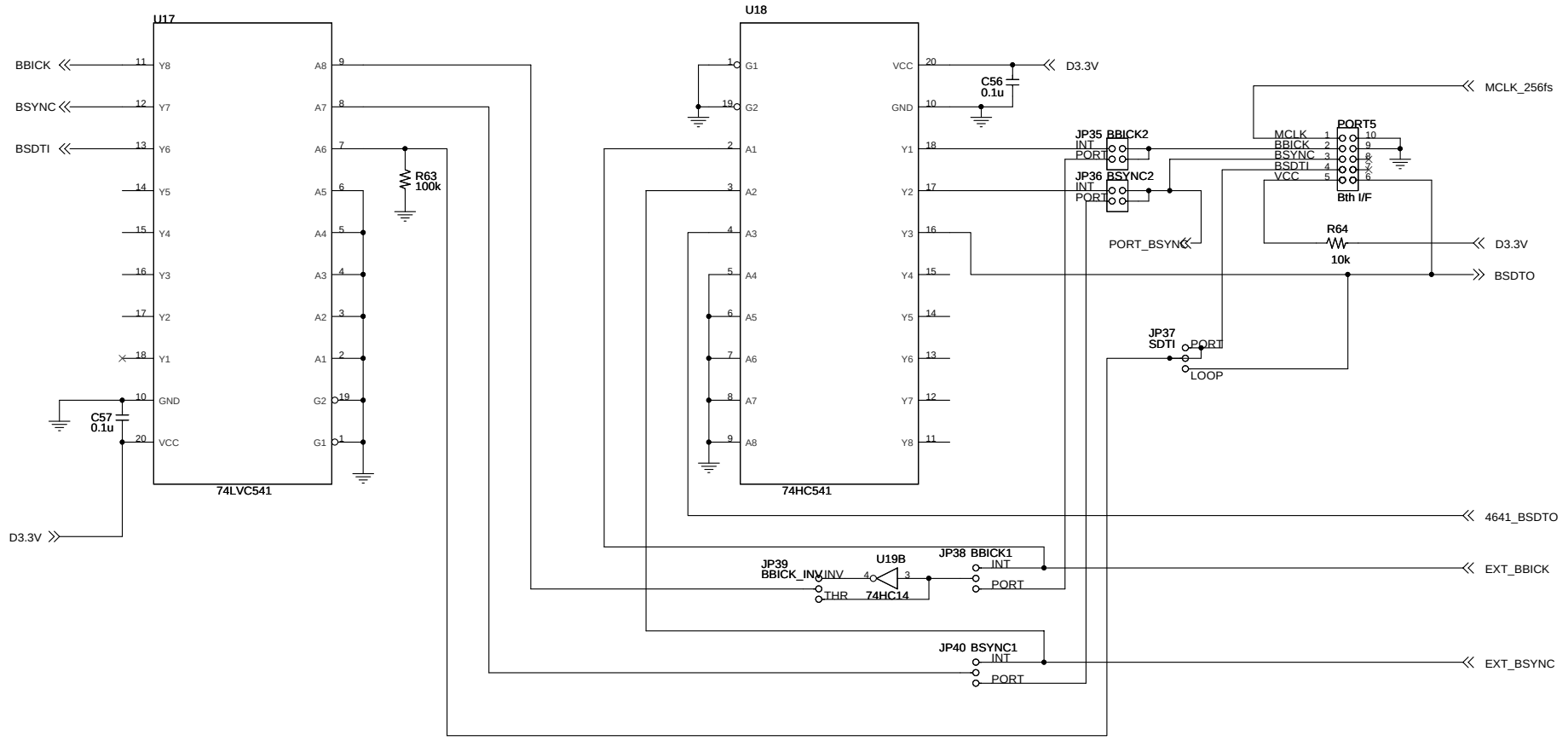
Title	AKD4641	
Size: A3	Document Number: Input/Output	Rev: A
Date: Friday, November 25, 2005	Sheet 2 of 6	

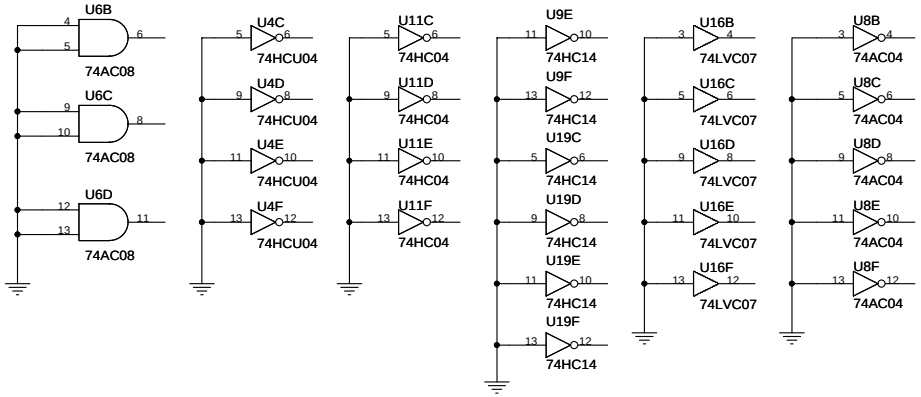


Title	AKD4641	
Size: A3	Document Number: CLOCK_Bth	Rev: A
Date: Wednesday, July 23, 2003	Sheet 3 of 6	



Title	AKD4641	
Size: A3	Document Number: LOGIC_AUDIO	Rev: A
Date: Wednesday, July 23, 2003	Sheet 5 of 6	





for
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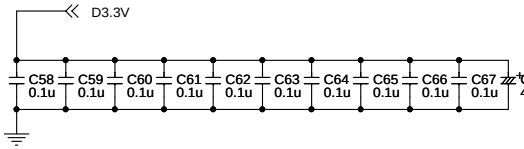
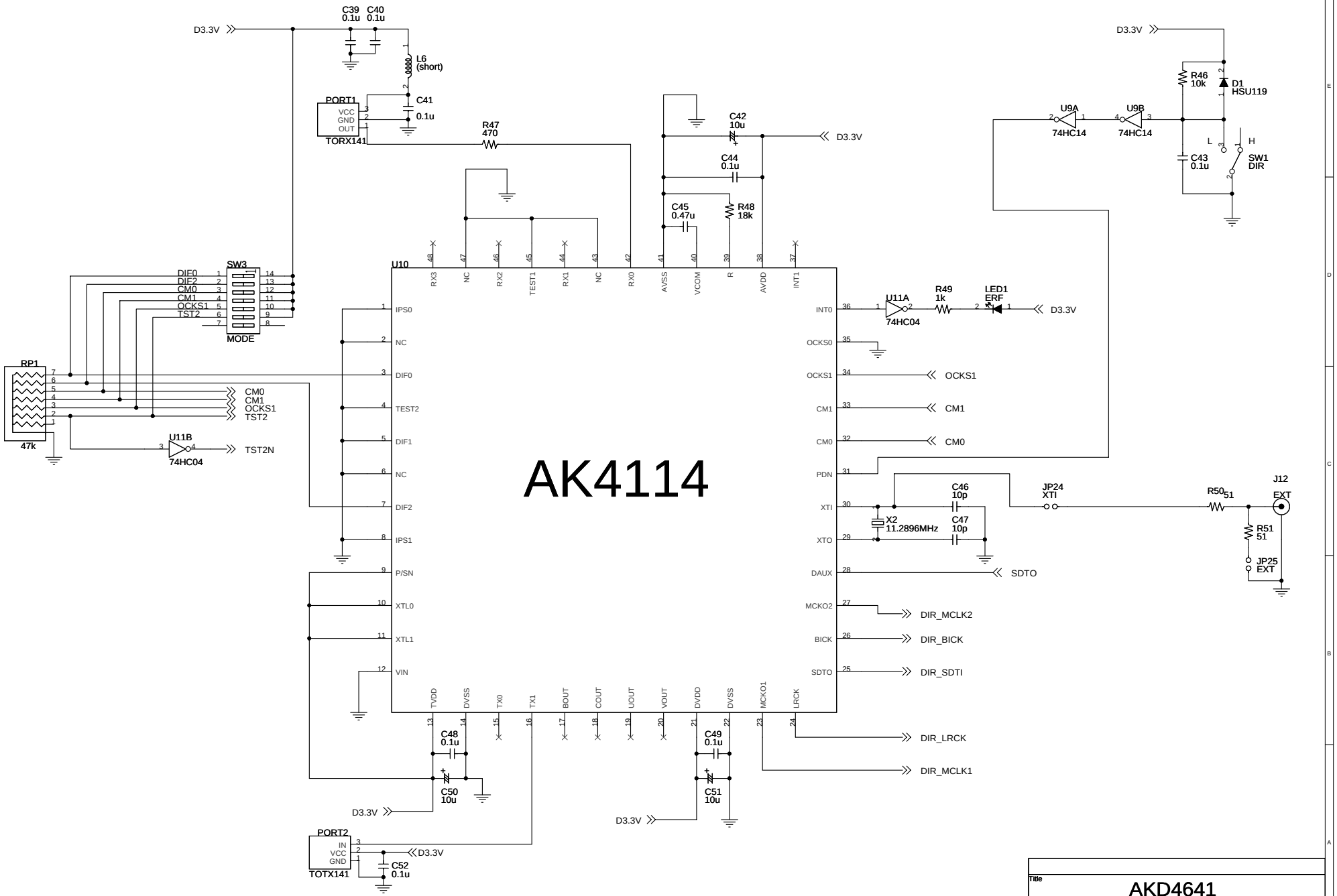


Title	AKD4641	
Size A3	Document Number LOGIC_Bth	Rev A
Date: Wednesday, July 23, 2003	Sheet 6 of 6	



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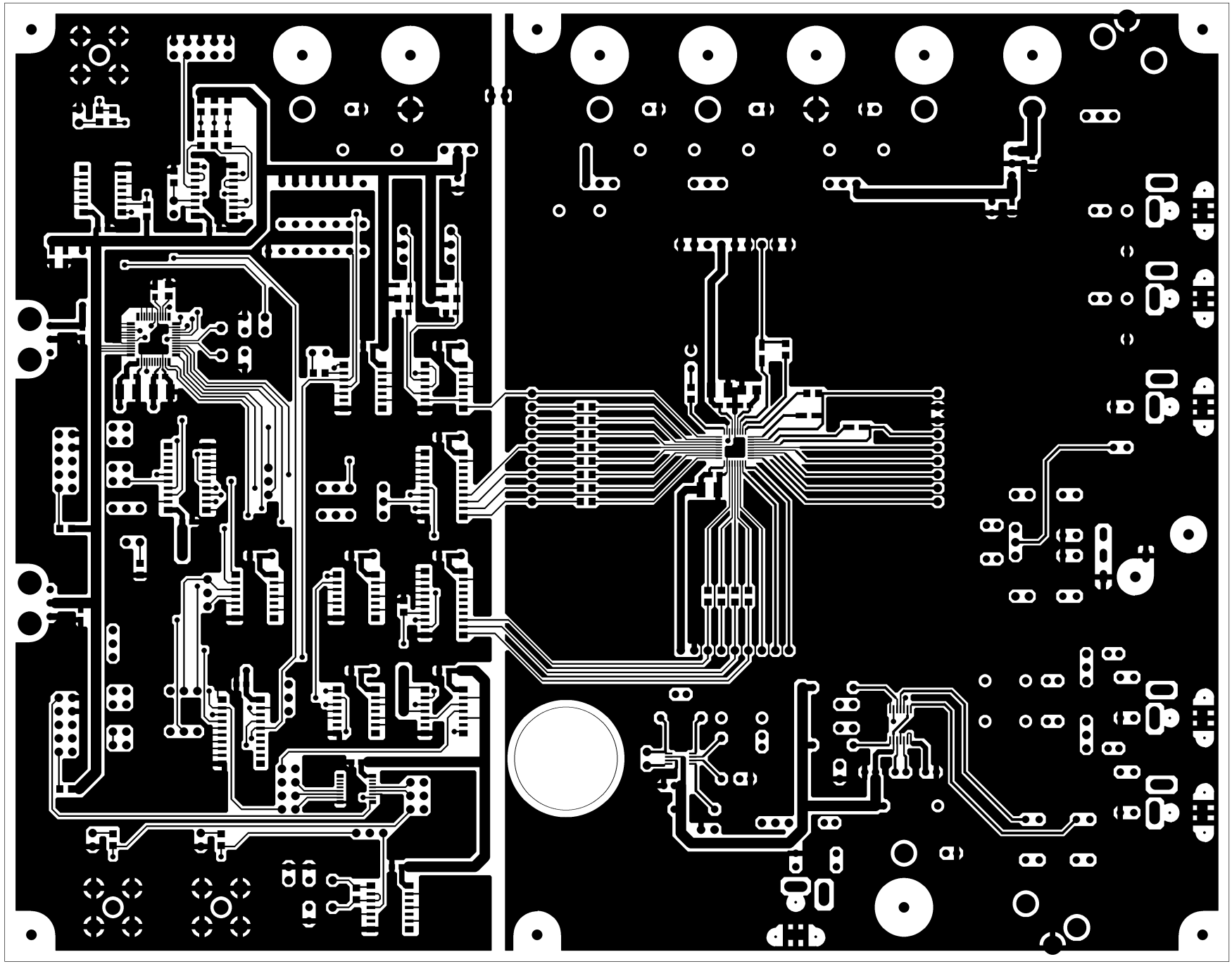
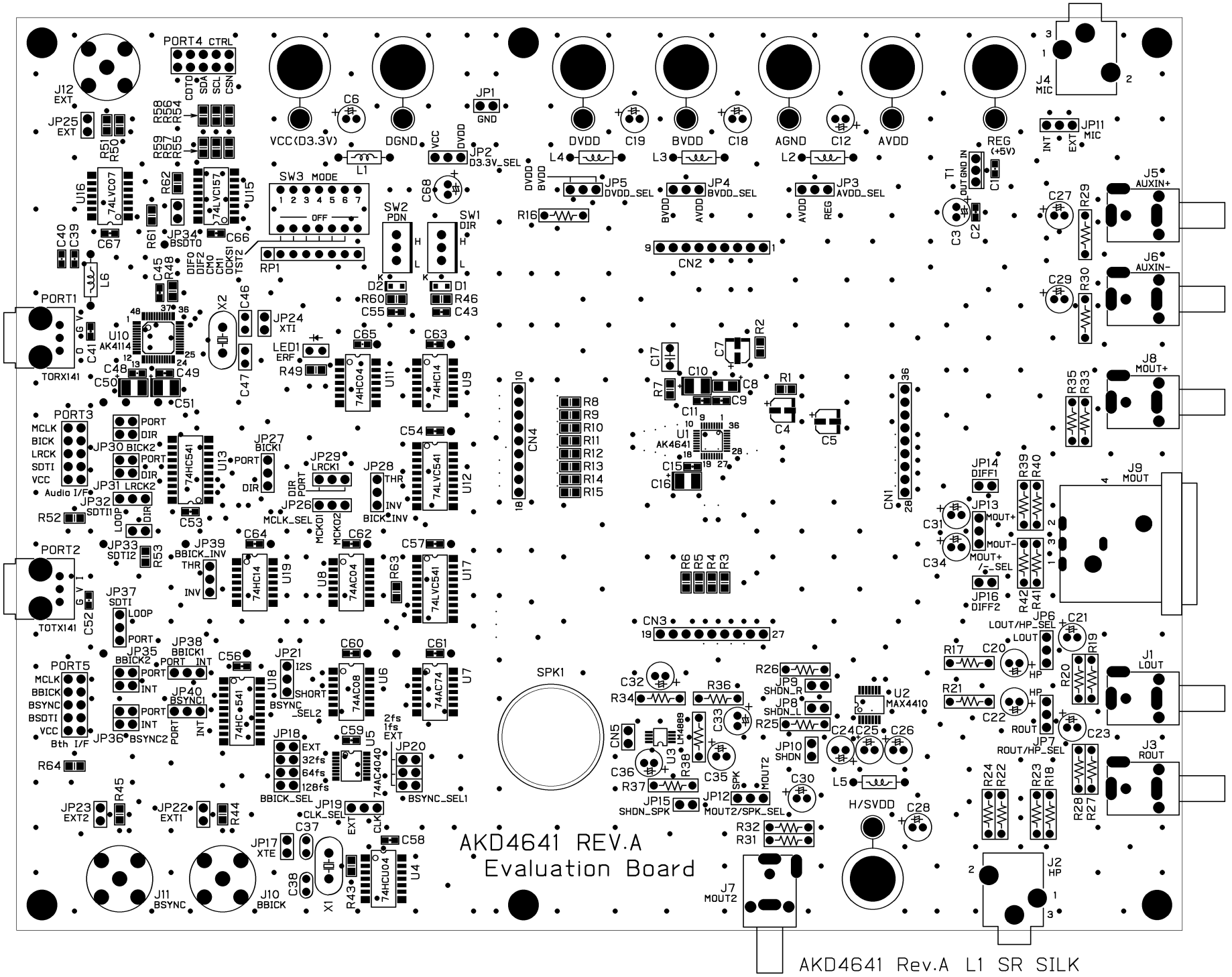
Size A3	Document Number DIR/DIT	Rev A
Date: Wednesday, July 23, 2003	Sheet 4 of 6	

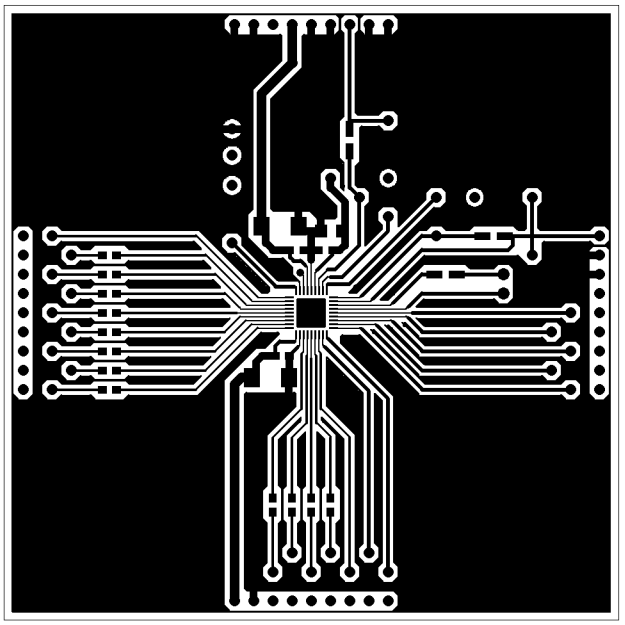


AKD4641 Rev.A L1

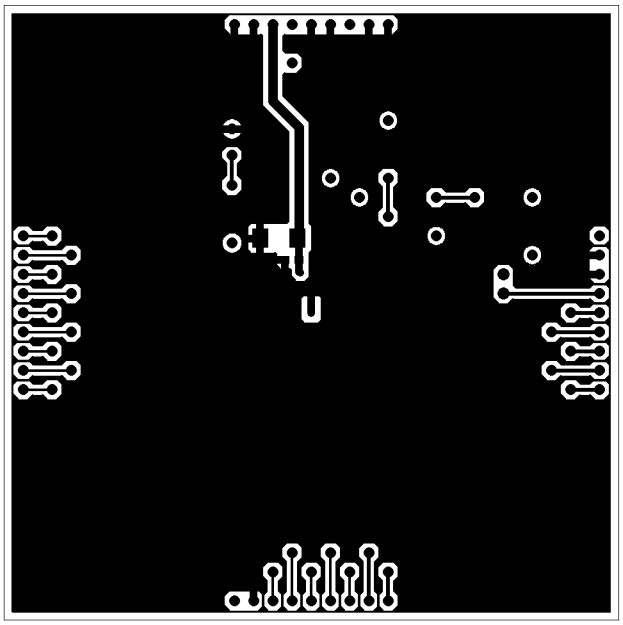
AKD4641 Rev.A L2


AKD4641 REV.A
Evaluation Board
AKD4641 Rev.A L1 SR SILK

AKD4641 Rev.A L2 SR SILK



L1 PATTERN



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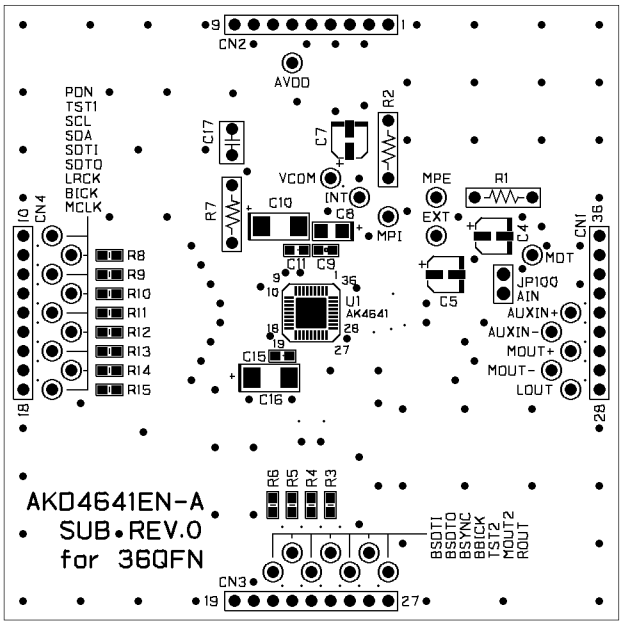
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R12
R13
R14
R15
C17
R7
C7
R2
VCOM
INT
C10
C8
MPI
C1
C9
U1
AK4641
C15
C16
MPE
EXT
R1
C4
C5
MDT
JP100
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AUXIN+
AUXIN-
MOUT+
MOUT-
LOUT
CN1
AKD4641EN-A
SUB•REV.0
for 360FN
R6
R5
R4
R3
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BSDTO
BSYNC
BBICK
TST2
MOUT2
ROUT
CN3

L1 S/R SILK

L2 S/R SILK